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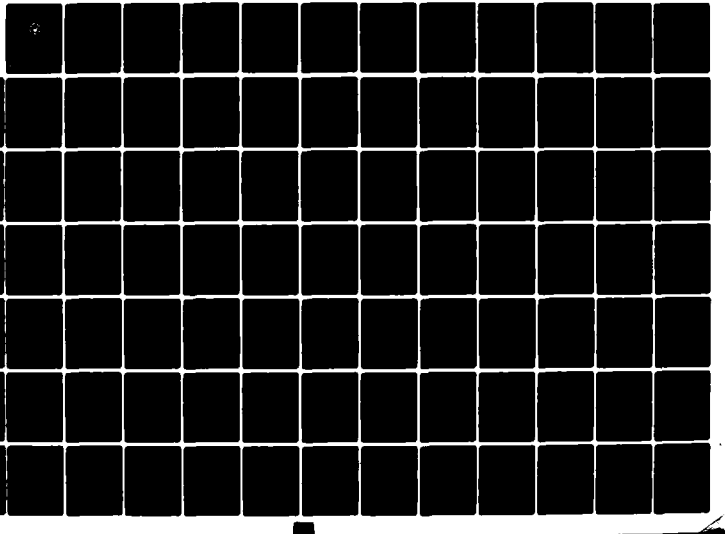

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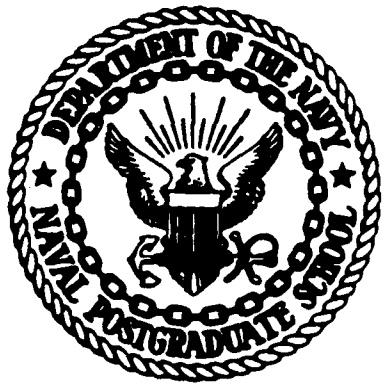

THESIS

DATA ACQUISITION SYSTEM FOR USE IN THE STUDY OF GEOMAGNETIC VARIATIONS

by

Hugh H. Thomas

December 1980

Thesis Advisor: R. Panholzer

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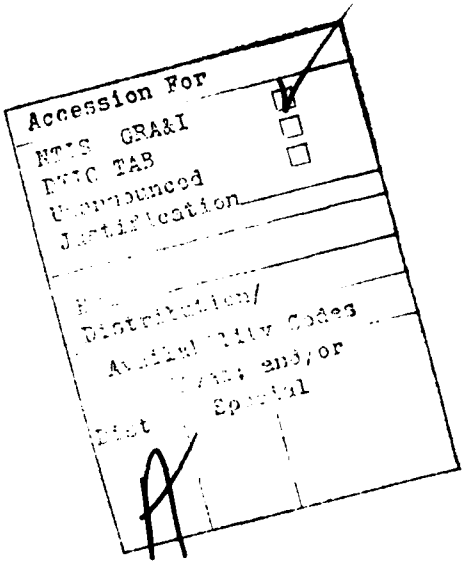
intermediate data memories are used; alternating between being written onto by the acquisition circuit and being read from for writing to the data recorder.



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Data Acquisition System For Use In
The Study of Geomagnetic Variations

by

Hugh H. Thomas
Captain, U. S. Army
B.S., United States Military Academy, 1975

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
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Author 

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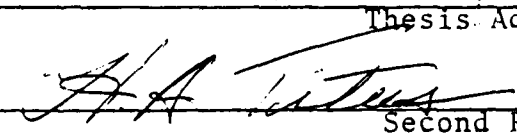
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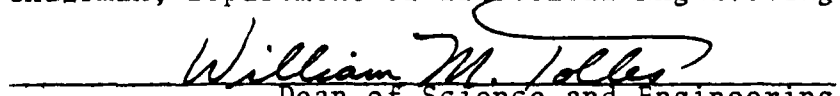
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ABSTRACT

The study of the variations in the geomagnetic field requires a small, low power digital data acquisition system. This thesis describes the design of a digital data acquisition system for such use. The design uses the complementary metal-oxide-semiconductor (CMOS) version of the INTEL 8048 single chip microcomputer and a high density data recorder. The microcomputers do not take data internally, instead they route data over a separate data bus. Two intermediate data memories are used; alternating between being written onto by the acquisition circuit and being read from for writing to the data recorder.

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I. INTRODUCTION

For the past four years a study of the variations in the spectral components in the earth's magnetic field has been carried on by the Physics and Chemistry Department at the Naval Postgraduate School. Data in this study has been taken primarily on the ocean floor off the Monterey, California coast and recently at remote land locations. The variations have been of a very low magnitude and predominantly in the frequencies of 100 Hertz or less. Variations in the ten Hertz or less region are of particular interest in this study.

To date, the data acquisition technique has been analog. The variations of the magnetic field are sensed by a magnetometer. The variations are frequency modulated by a voltage controlled oscillator and recorded on an analog recorder. This technique has been subject to the problems of the restricted data capacity of the analog recorder and excessive power consumption. These two problems have restricted data acquisition to a few hours or less at one time.

An alternative data acquisition technique is a digital system utilizing low power components and a high density digital recorder. The use of low power complementary metal-oxide-semiconductor (CMOS) components and a high density digital recorder of external dimensions to fit into a 17.5

inch diameter glass sphere for ocean floor observations is considered to be the best means of implementing this technique. The purpose of this thesis investigation was to design a digital data acquisition system for use in ocean floor observations and with minor modifications be adapted for land based observations. The acquisition system is designed to consume a minimum amount of power while providing as large a data capacity and as wide a range of observation as possible.

II. GENERAL CONCEPT

The acquisition system shown in Fig. 1, is to convert an analog voltage to a digital representation which is proportional to the geomagnetic field. This digital value is then placed into an intermediate memory. The intermediate memory must be large enough to allow an economical use of the data recorder. When this intermediate memory has been filled it is transferred to the data recorder. The control element determines when data is to be taken according to the Nyquist criterion, and controls the loading of the intermediate memory and the actions of the data recorder. Continuity in data acquisition is essential and is accomplished by providing two intermediate memories of equal size. While one memory is being filled with new data, the data in the second memory is being read and recorded. The use of the two intermediate memories also allows the data rate to be changed from the slow acquisition rate to the high data rate of the high density data recorder.

The control element is to exercise control over data routing, sampling, and input/output. This element is not intended to process data. To avoid restrictions of data word length the address bus and data bus are separate. The address bus provides addresses to the intermediate data memories. The data bus connects the ananlog-to-digital

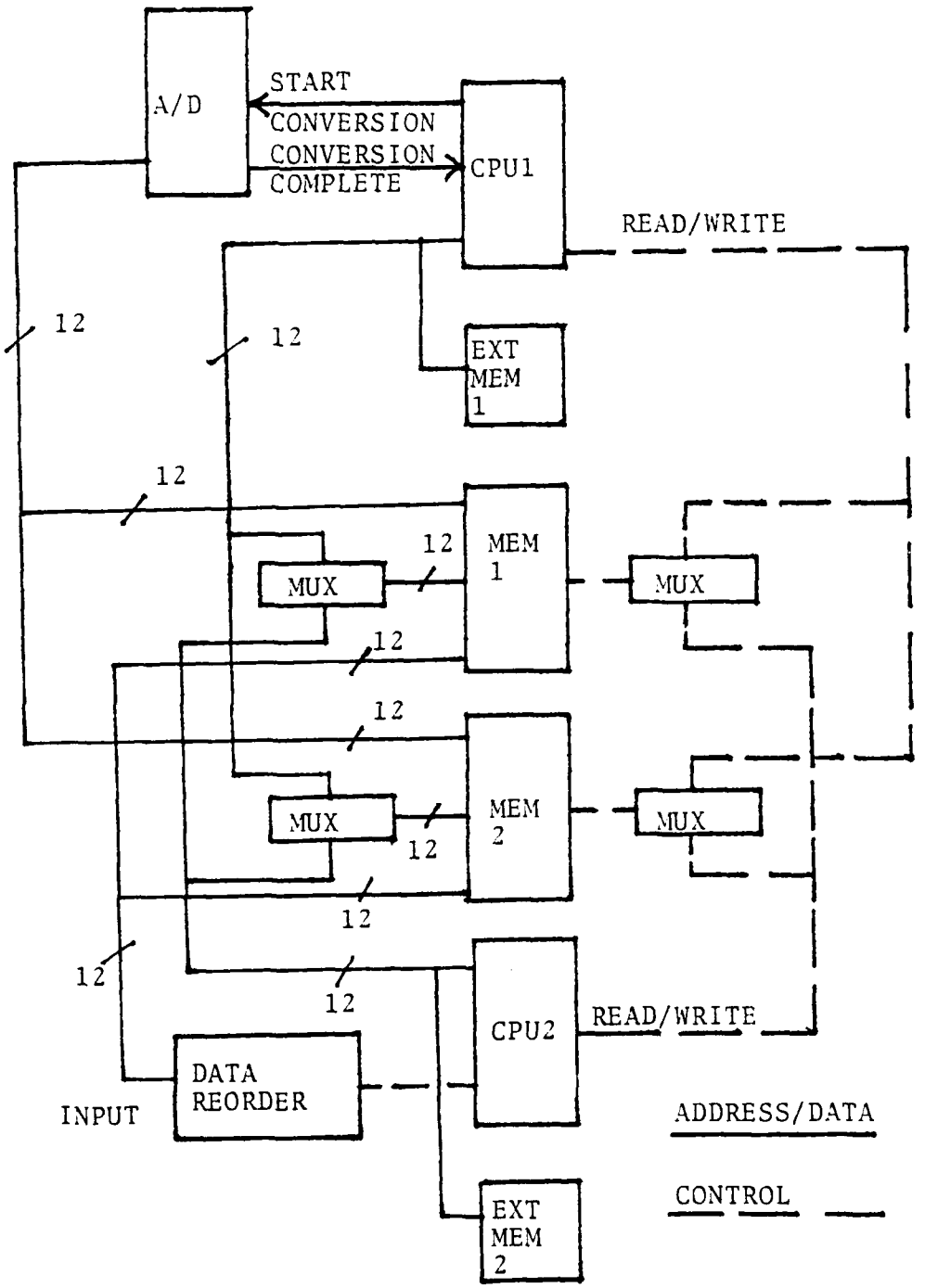


Fig. 1. System Block Diagram

converter to the memory, the memory to the data recorder, and the memory to the digital-to-analog converter. Data does not physically pass through the control element but is routed by the control element. This allows the data word length to be independent of the processor word length.

The control element is split into two parts. The first part, central processing unit one (CPU1), exercises control over the data acquisition and reconstruction phases. The second part, central processing unit two (CPU2), exercises control over the data recorder. To accomplish these control functions the INTEL Corporation Single Chip Microcomputer System, MCS-48 Family, 8748/8048 was chosen [1]. The 8748 and 8048 are single chip microcomputers with two eight bit input/output ports, one eight bit bus port, three status lines, and 64 eight bit random access memory (RAM) locations on chip. The 8748 provides one kilo byte, 1024 or 1k, of erasable programmable read-only-memory (EPROM) on chip for program storage. The 8048 provides 1k byte of on chip read-only-memory (ROM) for program storage. Both the 8748 and the 8048 allow for program and data memory off chip. The 8748 and 8048 are currently only available in metal-oxide-semiconductor (MOS) versions. The MOS versions consume too much power for this application, however low power CMOS versions of the 8048 are expected to be available from several sources in early 1981 [2]. Peripheral devices

to the control elements used in this design are currently available in CMOS or Low Power Schottky transistor-transistor logic (LSTTL).

The data recorder tentitively selected in the Series 3400 High Density Cartridge Magnetic Tape Drive, the Funnel, manufactured by Data Electronics Incorporated (DEI). The drive has a recording density of 6400 bits per inch, a serial transfer rate of 192 kilo bits per second, and a unformated capacity of 17.3 mega bytes. It is the tape drive that will be the primary consumer of power at approximately 18 watts. This drive was tentatively chosen for its small size and high data capacity. While it is not ruggidized, it is felt the drive will be able to withstand the temperature range on the ocean floor. Verification of this will require additional testing and is beyond the scope of this thesis.

The sampling period is determined by the internal time base of CPU1. When one sampling period has elapsed, the analog-to-digital converter (A/D) is signaled to acquire a sample. This digital sample is then stored in the intermediate memory. The design can accommodate eight 8 or 12 bit data by arranging an A/D of that width with that number of one bit wide static CMOS RAM circuits. This system is designed for 12 bit data words, The twelve address lines, eight bits from the bus port and four from one of the I/O ports, allow for 4096, 4k, data words to be stored in each

of the two intermediate memory blocks, The intermediate memory blocks are made up of 4k by one bit static CMOS RAM circuits. The selection of which block is to be filled is controlled by CPU1. The alternate block is available to CPU2 for reading and recording.

The reconstruction phase is activated by CPU1 signaling CPU2 to fill one block of memory from the tape. When one block has been filled, CPU1 begins reconstruction by reading the data and providing it to the D/A. While the D/A function is being accomplished, CPU2 is filling the alternate block of intermediate storage from the recorder. This read and reconstruction sequence is continued under the control of CPU1. Each time the reconstruction of the data just read from the tape is started by CPU1, CPU2 is signaled to read the next block of data from the tape, filling the alternate block. This method allows a continuous stream of analog data to be available at the output of the D/A.

III. HARDWARE

The hardware is split into three distinct functional areas: the data recorder, the controllers, and the intermediate memory. The intermediate memory is a universal part and will not be specifically addressed in this part of the thesis. The data recorder and the CPU's are very flexible devices, and a full explanation of their functions would be extremely long and beyond the scope of this thesis. Only those aspects specifically related to this design will be discussed.

A. THE DATA RECORDER

The data recorder used in this design is the DEI series 3400 Funnel recorder. The produce specification is provided as Appendix A. The control over the device is excercised by CPU2. All control signals for the data recorder are TTL compatible. Its data transfer rate, 5.2 msec per bit, is compatible with the 8748 or 8048 used in CPU2.

The data recorder can be acquired in several different configurations from the manufacturer. The basic model was chosen for this design due to power considerations. The alternative configurations included a control card or a combination of the control card and a codex card. The additional cards boost power consumption by themselves by

more than one watt. In addition, the control care includes a feature that automatically rewinds the tape to its physical beginning when power is applied to the data recorder. This rewind function and the required search for the last block recorded would consume excessive quantities of power. For this reason, these cards were not included in the design. This choice required an interface circuit to be designed to encode and decode the Modified Frequency Modulation (MFM) code, referred to also as the Miller or delay code, used by the data recorder. The code, as shown in Fig. 2, represents a "1" as a transition at the mid-bit period. A "0" is encoded as a transition at the beginning of the bit period unless preceeded by a "1", in which case no transition takes place.

The tape cartridge used with the data recorder is American National Standards Institute (ANSI) standard X3.56-1977 compatible, see Fig. 3. The upper and lower tape holes provide indications of tape position. The drive senses the presence of these holes and provides this information as output control signals. The recorder format specifies an interblock gap of 1.2 inches to get the tape completely stopped after one block and completely started to the read/write speed for the next block. The data block consists of a preamble of 39 "0's" and one "1" followed by the data and a postamble of 39 "0's". Using this format the tape capacity is 193.44 mega bits, 86 percent of the

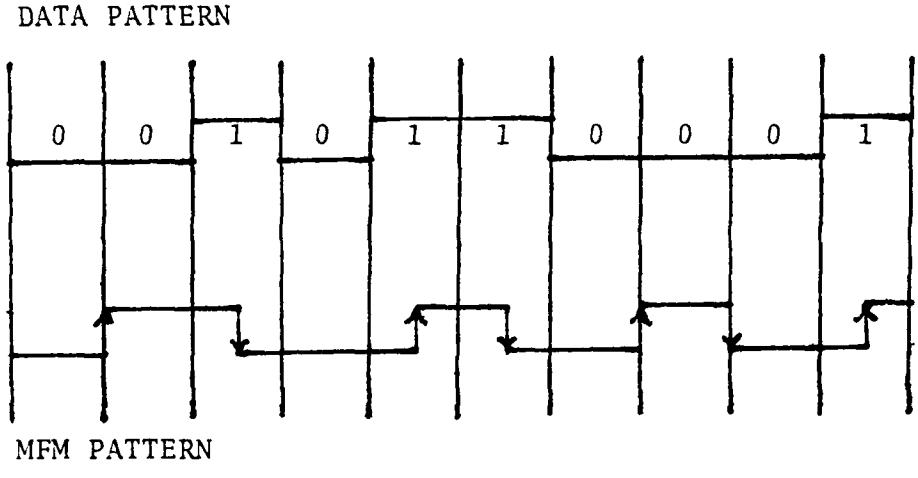


Fig. 2. Modified Frequency Modulation (Miller Code)

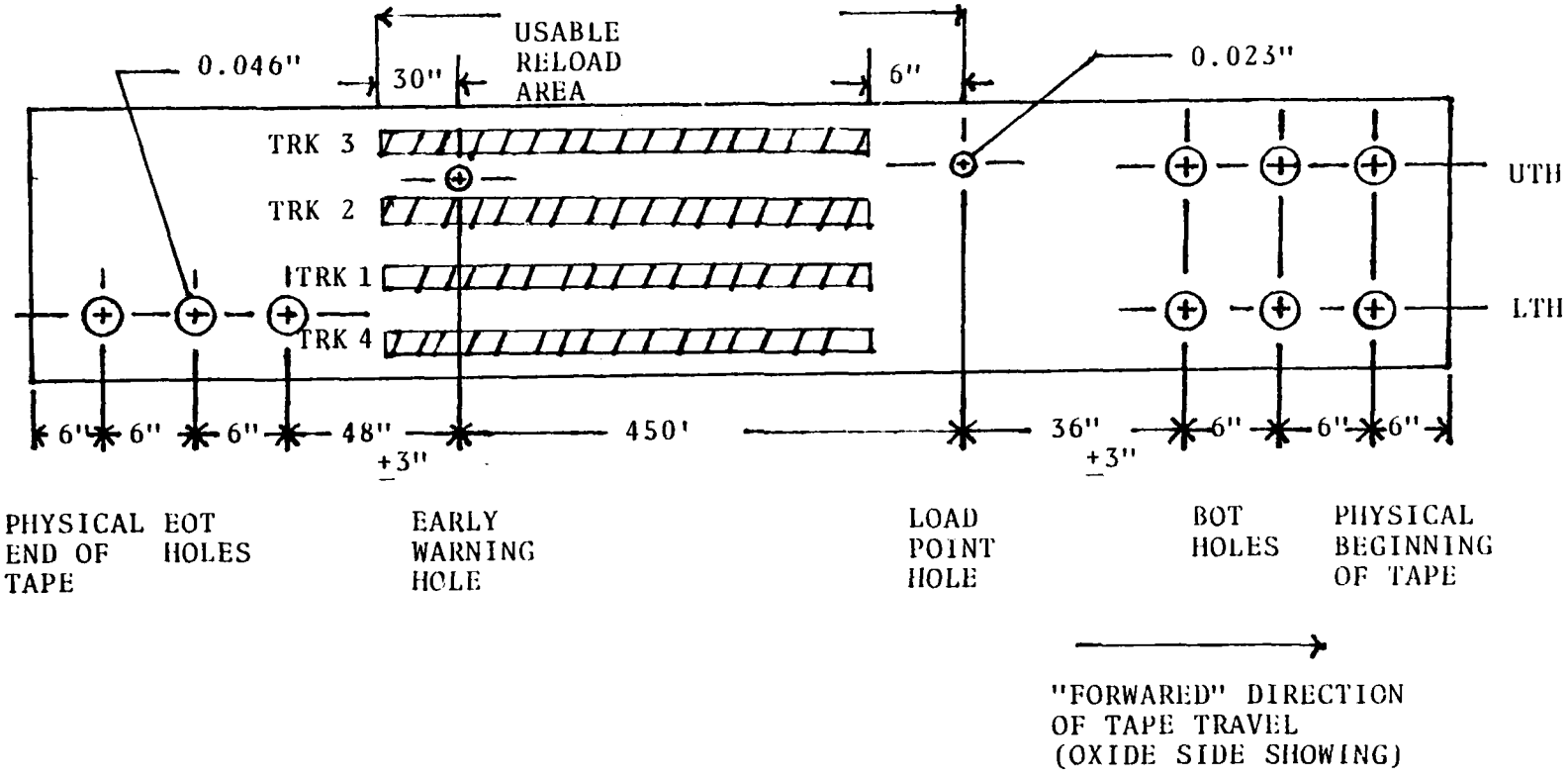


Fig. 3. ANSI Standard X3.55-1977

unformated capacity. The transfer time at the 30 inches per second read/write speed for one block is 258.5 msec.

The signals associated with the basic drive are listed in section 5.1 of Appendix A. The "-" indicates active low signals and the "+" active high signals. If both a + and - are shown, both an active high and active low signal are available.

B. 8048/8748

The 8048/8748 is the eight bit single chip microcomputer produced by INTEL Corporation [1]. The timing cycle of the device is derived from the external crystal. This basic frequency can range from 1 MHz to 6 MHz. The timing state is derived by dividing this frequency by three. Each instruction cycle consists of five states. The Address Latch Enable (ALE) output clock is derived by dividing the state frequency by five. This time derivation is shown in Fig. 4. The instruction set consists of either one or two cycle instructions stored as one or two bytes in program memory. A complete listing of the instruction set can be seen in Ref. 2.

The forthcoming CMOS version of the single chip microcomputer will be the ROM verions 8048. This will require an external program memory. The result of going to the external program memory is the addition of one instruction cycle to fetch the instruction and an additional cycle to

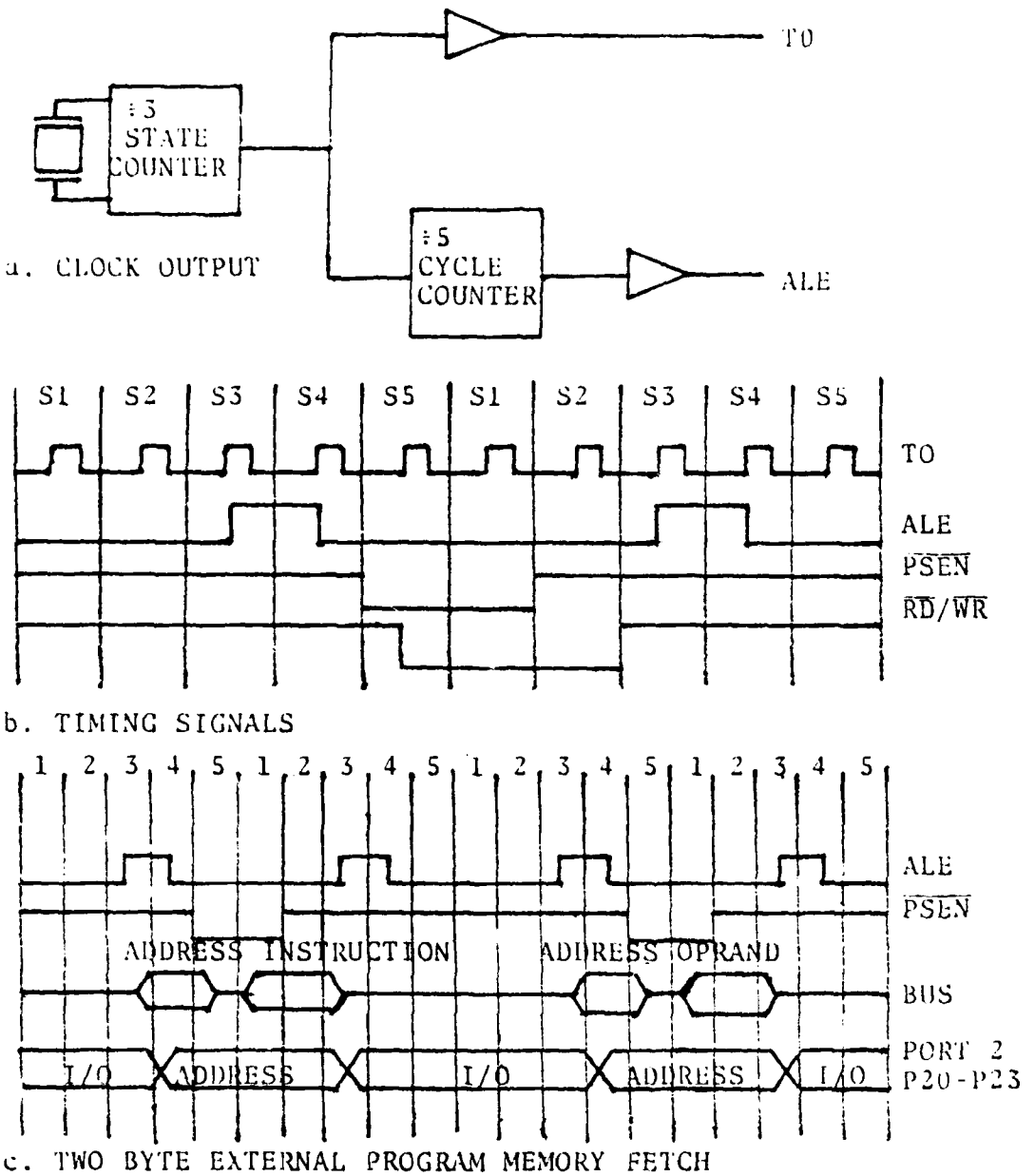


Fig. 4. CPU Timing Diagram [1]

fetch the operand when necessary. The 12 bit program counter is output on the bus port (P0) and the lower half of P2. The eight bit instruction or operand is returned to P0. Figure 4 shows the external program memory fetch cycle.

IV. THE CIRCUIT

The design dictates the system be divided into two circuits, the acquisition circuit and the reconstruction circuit. There are 4096 sample periods per block period. A sampling interval is a period of continuous data collection timed by the number of blocks taken in the interval. The non-sampling interval is the time when no data is being collected, or the period between sampling intervals.

A. THE ACQUISITION CIRCUIT

The data acquistion circuit is designed for 12 bit data using a 12 bit A/D and two 4k by 12 bit intermediate memories. The control elements are CMOS 8048's.

1. The Analog-to-Digital Converter

The analog-to-digital converter chosen for the design is the Intersil ICL 8068/7104-12 CMOS 12 bit A/D chip pair. The device is an integrating type A/D with a maximum conversion rate of 48 conversions per second [3]. The 8068/7104-12 pair was chosen for its low power consumption, TTL compatibility with no interface requirements, and a wide voltage range. The relatively low conversion rate is well within the Nyquist rate for the frequency range of interest.

The A/D will be operated in a convert or demand basis. CPU1 will signal for start conversion. The conversion complete signal will vector the program controling CPU1 to the interrupt service routine, thereby storing the data. The device is connected as shown in Fig. 5.

The voltage of the reference voltage (V_{ref}) determines what will be the full scale reading according to $V_{max} = V_{ref} \times 2$. For a 0 to 5 volt swing $V_{ref} = 2.5$ volts DC. The reselution of the 12 bit conversion over the 0 to 5 volts is .0244 per cent or 1.22 mV. The full 12 bit resolution of the A/D is accomplished by the addition of a polarity bit output by the device. When used it would give 13 bit resolution over a -5 to +5 volt swing.

When a sampling period was elapsed, the start conversion output from CPU1 makes a high to low to high transition to the RUN/$\overline{\text{HOLD}}$ pin. The status line goes high indicating a conversion is in progress. When the conversion is complete, the status line goes low triggering a 74LS122. The output of the 74LS122 provides the interrupt signal to CPU1. The low level of the status line also enables the output to the data bus. The output is now available to the memory for storage.

2. The Intermediate Data Memory

The intermediate data memory is made up to two blocks of 4096 by 12 bit static CMOS RAM. The 12 bit width is made up of 12 Intersil IM 6504 4k by 1 bit Static CMOS

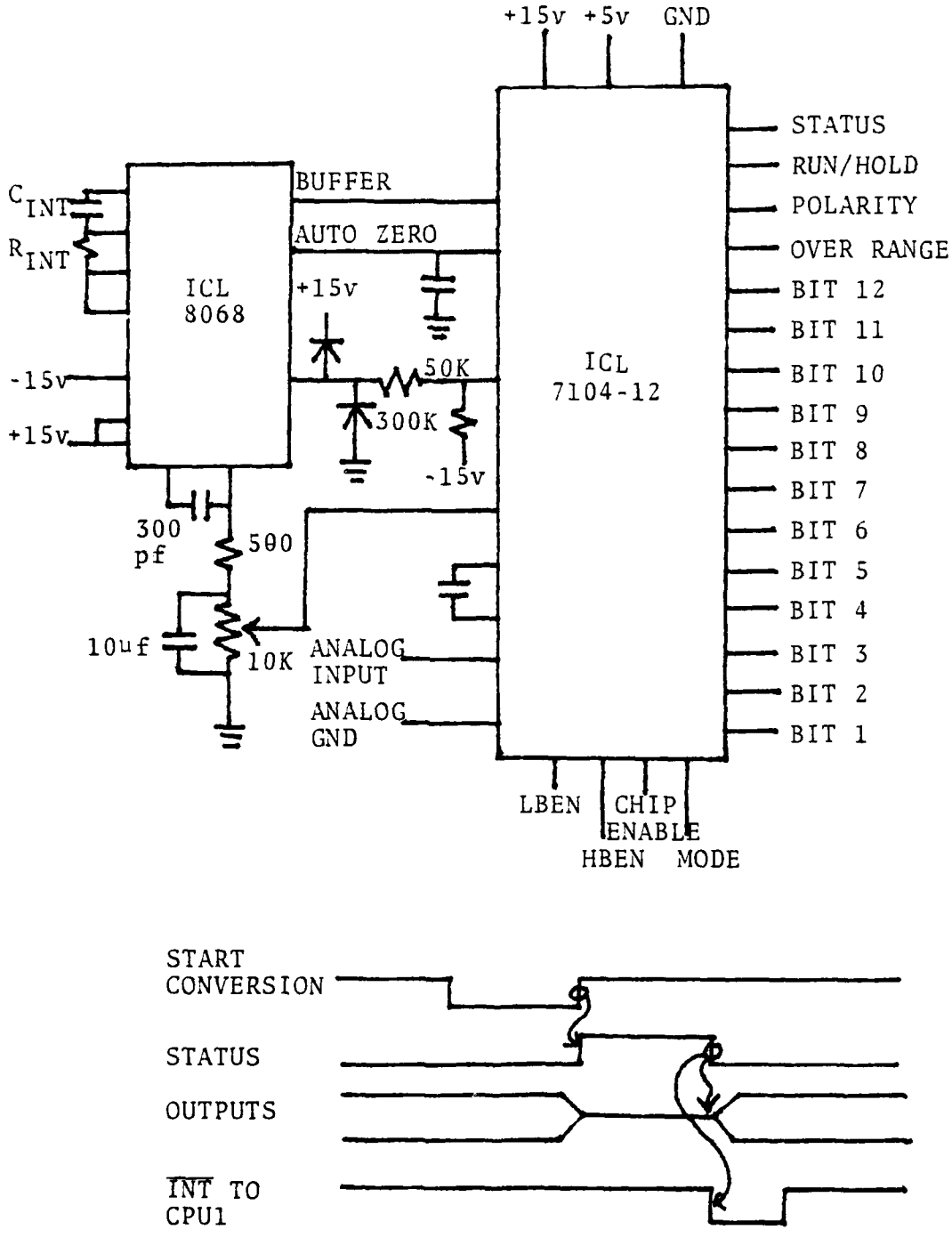


Fig. 5. Analog to Digital Converter [3]

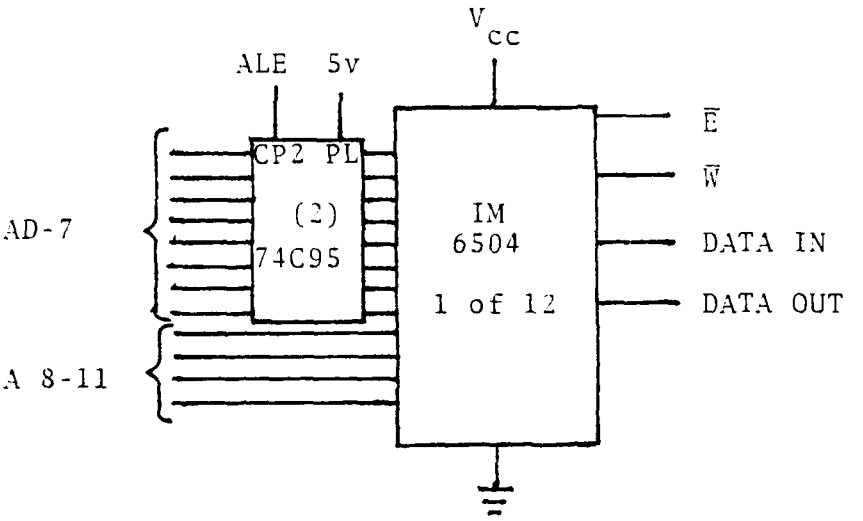
RAM circuits [5]. The circuit diagram is shown in Fig. 6. Due to the timing in the devide the lower eight bits of the address will have to be latched externally on the high to low transition of the ALW pulse. The read and write signals are used to generate the chip enable. The write enable is tied to the appropriate level at the inputs of the control multiplexers.

3. Multiplexed Data Pathes

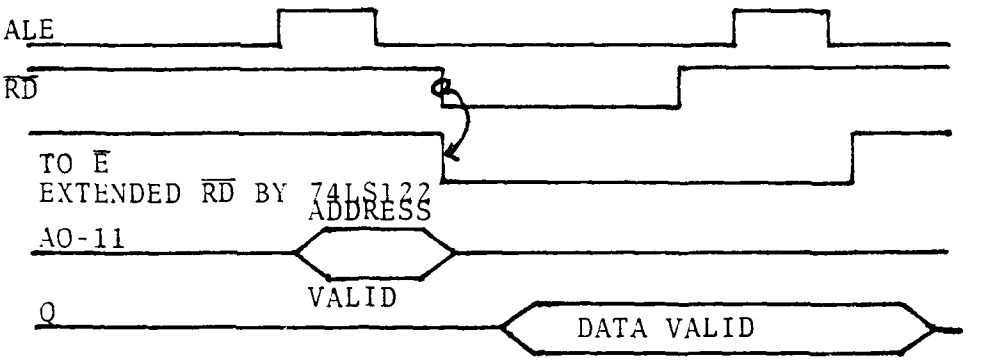
The CMOS 74C157 Quad 2-input Multiplexer is used to route control signals, addresses and page numbers to the proper intermediate memory from both CPU1 and CPU2, as shown in Fig. 7. The select line determines which set of four inputs will be gated through to the four outputs. The inverting of the select signal to the multiplexers associated with the second intermediate memory allows one of the intermediate memories to be available to CPU2 during the entire acquisition time. The power to the multiplexers will be from the same source as CPU1.

4. The Non-Sampling Interval Timer

The non-sampling interval timer consists of two Intersil ICL 8240 Programmable Timer/Counters [3]. The device and circuit is shown in Fig. 8. The time base is established by the resistor-capacitor network and is programmed by the dual inline package (DIP) switch. When activated by a low to high transition on the trigger the output goes low and stays low for the count on the DIP

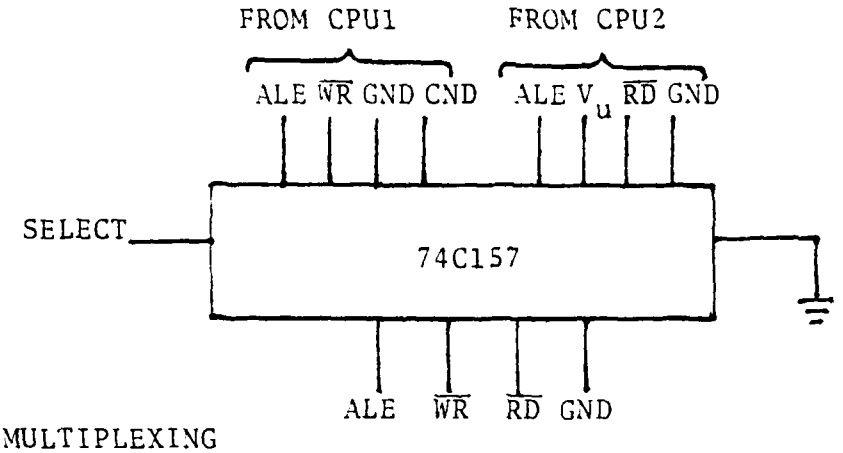


a. THE DEVICE

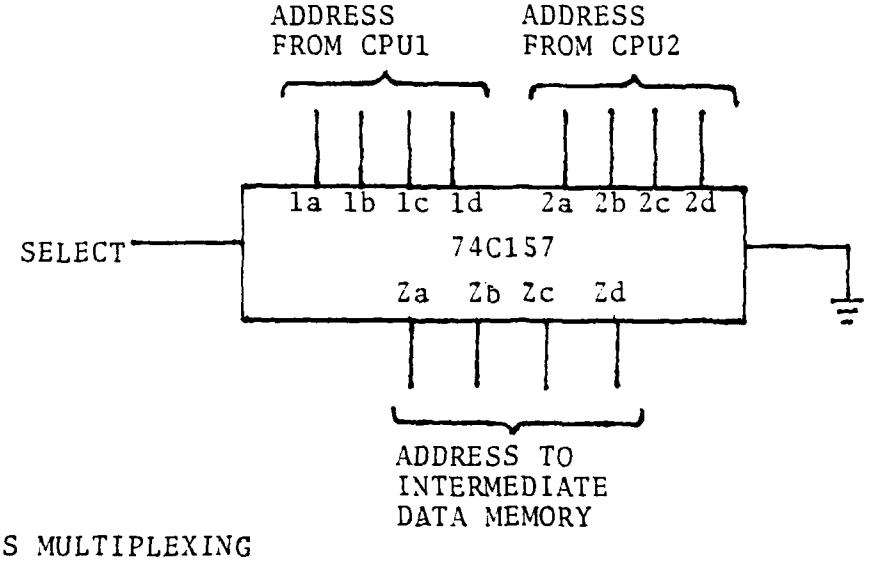


b. TIMING DIAGRAM FOR A READ CYCLE

Fig. 6. Intermediate Data Memory

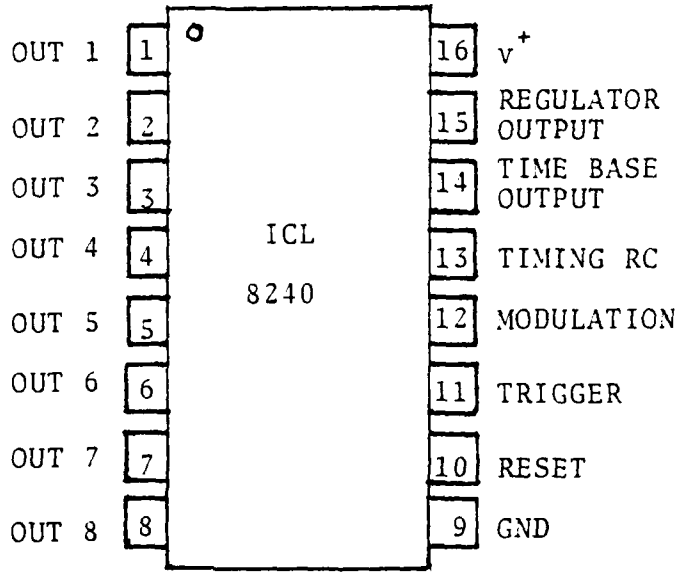


a. CONTROL MULTIPLEXING

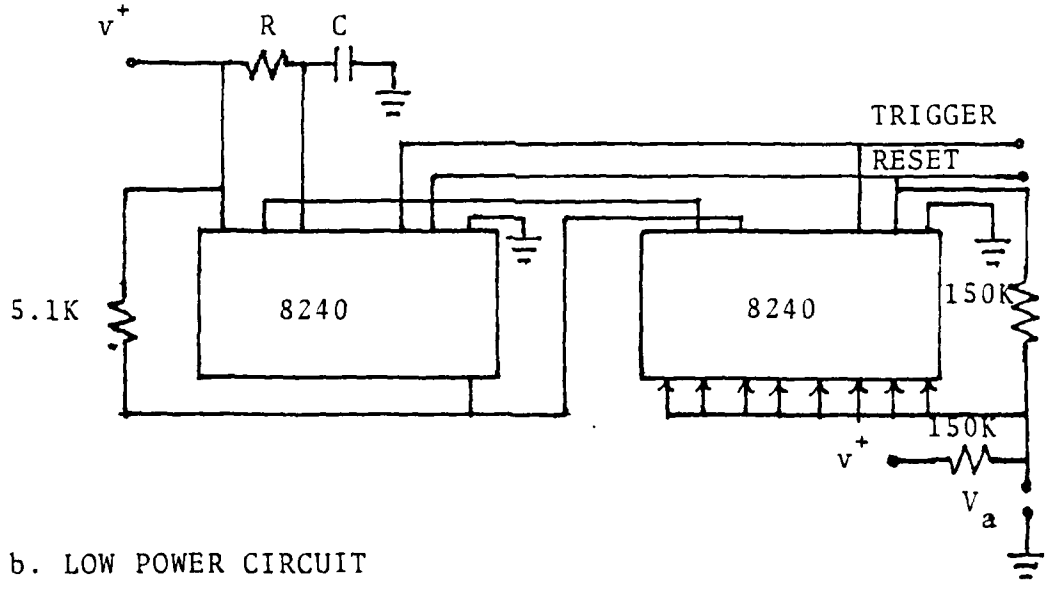


b. ADDRESS MULTIPLEXING

Fig. 7. Control and Address Multiplexing



a. THE DEVICE



b. LOW POWER CIRCUIT

Fig. 8. The Non-Sampling Interval Timer [3]

switch times the product of the resistor and capacitor. The output then goes high activating CPU1. The device is triggered by CPU1 at the end of a sampling interval. Power is left on continuously.

5. Central Processing Unit One

CPU1 controls the data acquisition function for the system. The device will be a CMOS version of the INTEL 8048 with an external program memory [1]. One version of the CMOS 8048 is the Intersil 80C48 [3]. The preliminary information indicates the 80C48 will be pin for pin compatible with the INTEL 8048 with virtually the same performance specifications. With CMOS logic, power consumption is directly related to speed of operation. For this reason and the desire to simplify the sampling control, a lower clock speed is desired. An external 3 MHz crystal will generate an instruction cycle of five micro seconds. This rate consumes less power and reduces the dividers needed to generate the sampling period from two to one. The device and circuit is shown in Fig. 9.

The bus port (PO) passes addresses to the intermediate data memory and the external program memory and receives instructions and operands from the external program memory. The lower half of P2 is dedicated to passing the most significant nibble, bits eight through eleven, of the program counter to the external program memory. P1 serves two functions. First, it provides an input port to the

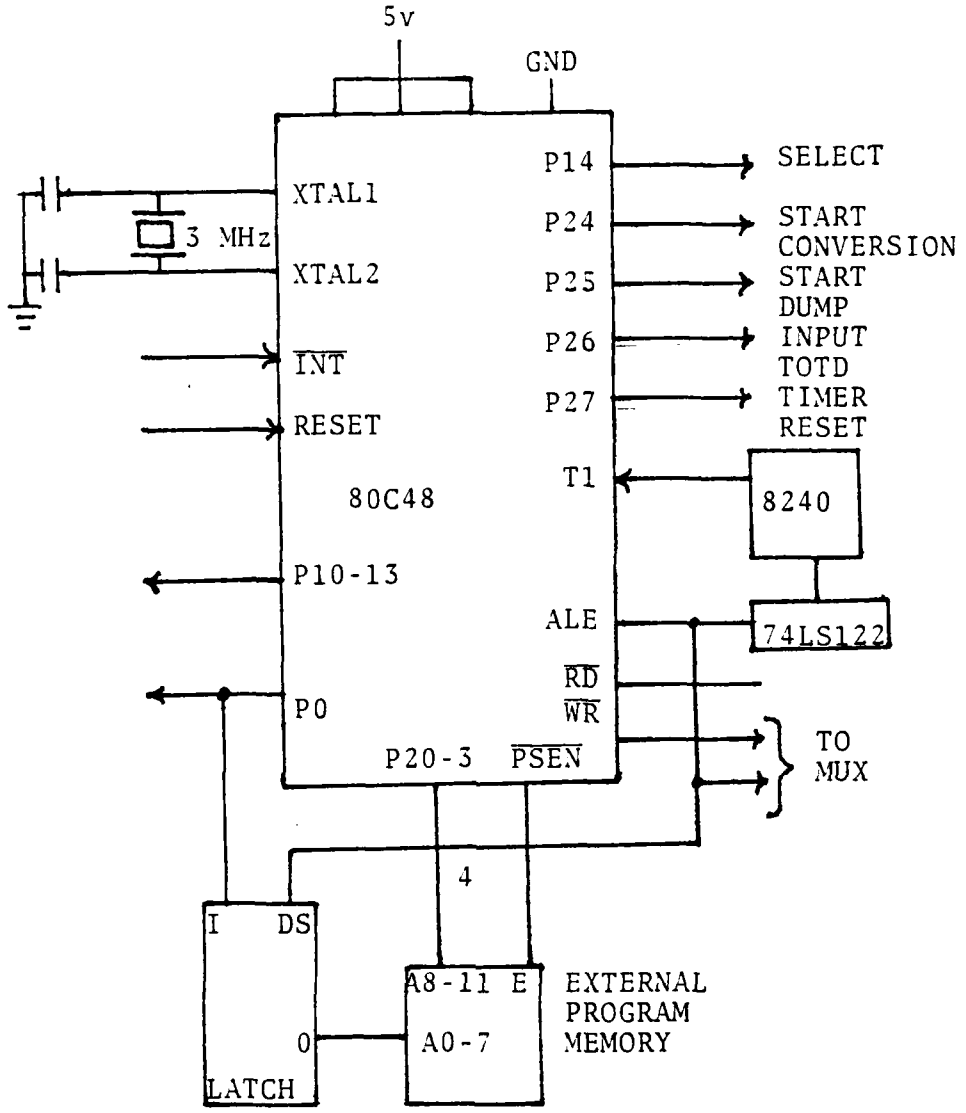


Fig. 9. CPU1 Acquisition Circuit

eight bit DIP switch that represents the number of data blocks to be taken during a sampling interval. Second, it outputs the four bits of the page number in the lower half and the select to the routing multiplexers on the first bit of the upper half. The external interrupt ($\overline{INT}$) is enabled under program control and is activated when a conversion has been completed by the A/D.

The Address Latch Enable (ALE) signal is used by the external program and data memories and is a time base for the sampling period timer. The sampling period is controlled by an ICL 8240 connected as shown in Fig. 10. The ALE signal is used as an external time base for the 8240. This time base is divided down according to the setting on the eight bit DIP switch connected to it. The ALE pulse width is not wide enough to be directly connected to the 8240. The pulse is widened by connecting the ALE signal to the trigger of a 74LS122 Retriggerable Monostable Multivibrator as shown in Fig. 10. The 8240 is programmed to divide the ALE signal down to the point where 256 pulses constitutes one sampling period. The output of the 8240 is fed into T1 of CPU1. When a count of 255 has been reached the event counter overflows and an interrupt routine signals for start conversion. The relationship for programming the 8240 is:

$$Y = \frac{F \times X}{256}$$

F = the frequency of ALE
X = the sampling period
Y = the number of the DIP switch

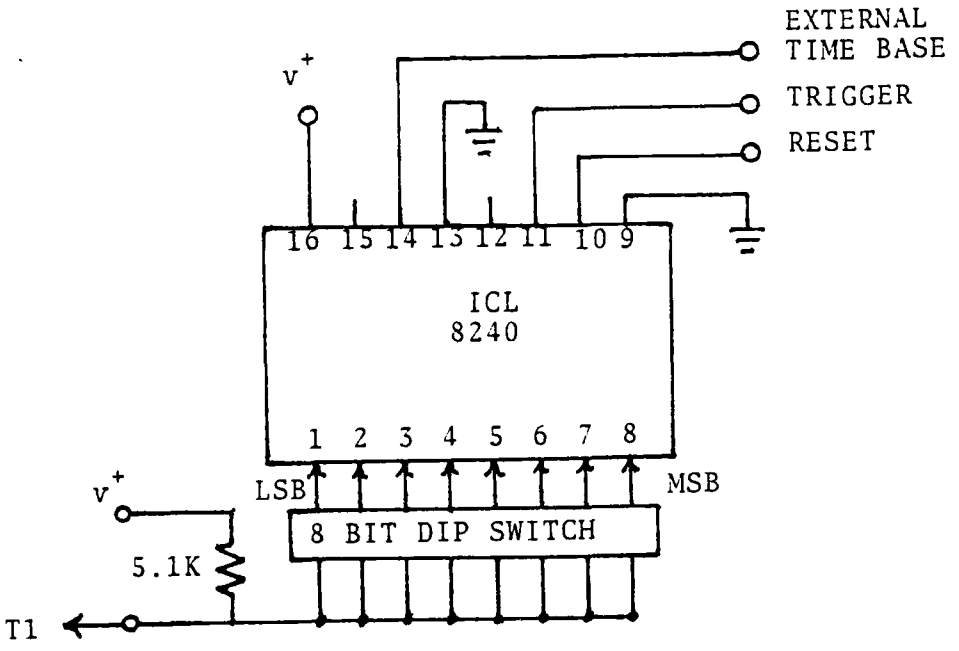


Fig. 10. Sampling Period Timed [3]

In the case of a 3 MHz crystal attached to the 80C48, ALE has a frequency of 200 KHz. If a sampling period of 200 msec, 5 Hz, is desired, Y = 156.25. This will be set into the DIP switch as 156 giving a sampling period of 199.68 msec, 5.0008 Hz.

The sixth line of P2 (P26) controls the input of the number of blocks to be taken during the sampling interval. This line is brought low under program control, and the contents set into the DIP switch can be input to CPU1. The start conversion signal is P24. It is brought low at the end of 256 counts on the event counter. The start dump signal, P25, brings power up to CPU2 and the data recorder, and resets CPU2 when a block of intermediate data is ready to be written to the data recorder. The signal is held low for the prescribed time required to reset CPU2. The select line, P14, controls the data routing multiplexers. When low, intermediate memory one is avaliable to CPU1 and intermediate memory two is available to CPU2. When high, the CPU's switch memories. The non-sampling interval timer is reset by P27. The line is brought low then high again. It is the low to high transition that activates the timer and shuts down the acquisition circuit. The non-sampling interval timer is reset to shut down the acquisition circuit after a sufficient amount of time has elapsed for CPU2 to have completed the transfer of the last block of data to the data recorder.

The external program memory consists of one 512 by eight bit EPROM. The Intersil IM 6654 CMOS 512 by 8 bit EPROM is used in this design, as shown in Fig. 11.

6. Central Processing Unit Two

CPU2 for the acquisition circuit is a CMOS 8048. The clock will be set to allow two instruction cycles per bit period of the data recorder. The minimum bit period of the DEI Funnel recorder is 5.2 micro seconds. This dictates the use of a crystal that allows no less than 2.6 micro seconds per instruction cycle. The commercially available 5.7143 MHz crystal will provide an instruction cycle of 2.625 micro seconds, extending the bit period of the recorder by 50 nano seconds. The circuit is shown in Fig. 12.

The bus port performs the same functions as in CPU1. P1 and the upper half of P2 perform two functions. The first function is control signal output. The second function is to input and output the current track and the number of blocks recorded on that track. This information is essential in accounting for the amount of data on the particular track in use to prevent the attempt at writing off the physical end of the tape. The lower half of P2 provides the external program memory with the most significant nibble of the program counter and outputs control signals. This double duty requires the external latching of the control signals on the low to high transition of the

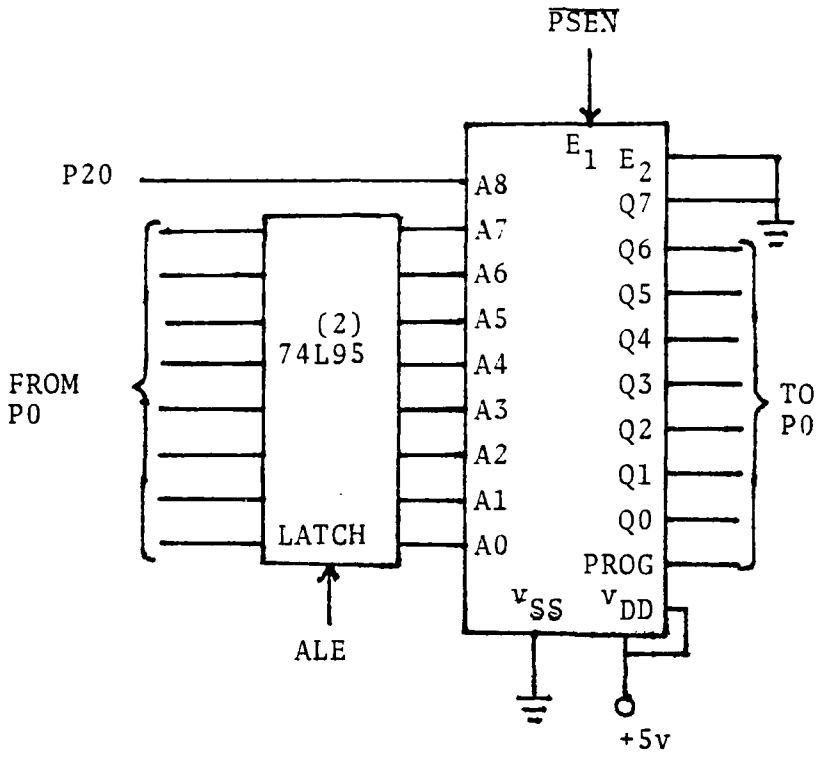


Fig. 11. External Program Memory IM 6654

ALE signal into a 74C175 Quad D Flip-Flop, as shown in Fig. 12. TO is used to detect the upper tape hole. The external interrupt is used to sense the lower tape hole. T1 is used to sense the data detect signal from the data recorder.

The twelve control lines originate from the upper half of P1 and all of P2. The upper half of P2 controls the track select and the tape motion. P24 and P25 provide the data recorder with the two bit track code. P26 and P27 are the active low forward and reverse signals, respectively. P23 will be used to trigger the time base for the shift register and the MFM encoder. P20 is used to shut down the power supplies to the CPU and the data recorder. P15 triggers a "1" to be written to the data recorder after the 39 "0's" of the preamble. P14 selects the data recorder allowing it to respond to input signals. P16 signals for high speed tape motion at 90 inches per second.

The control signals from P21 and P22 control the reading and writing functions for the track and block count storage. Each track can accomodate 606 data blocks. The number of blocks per track requires 10 bits with the track code requiring two bits. The twelve bits must be stored at all times during the acquisition phase to account for the track in use and the amount of tape used. The storage

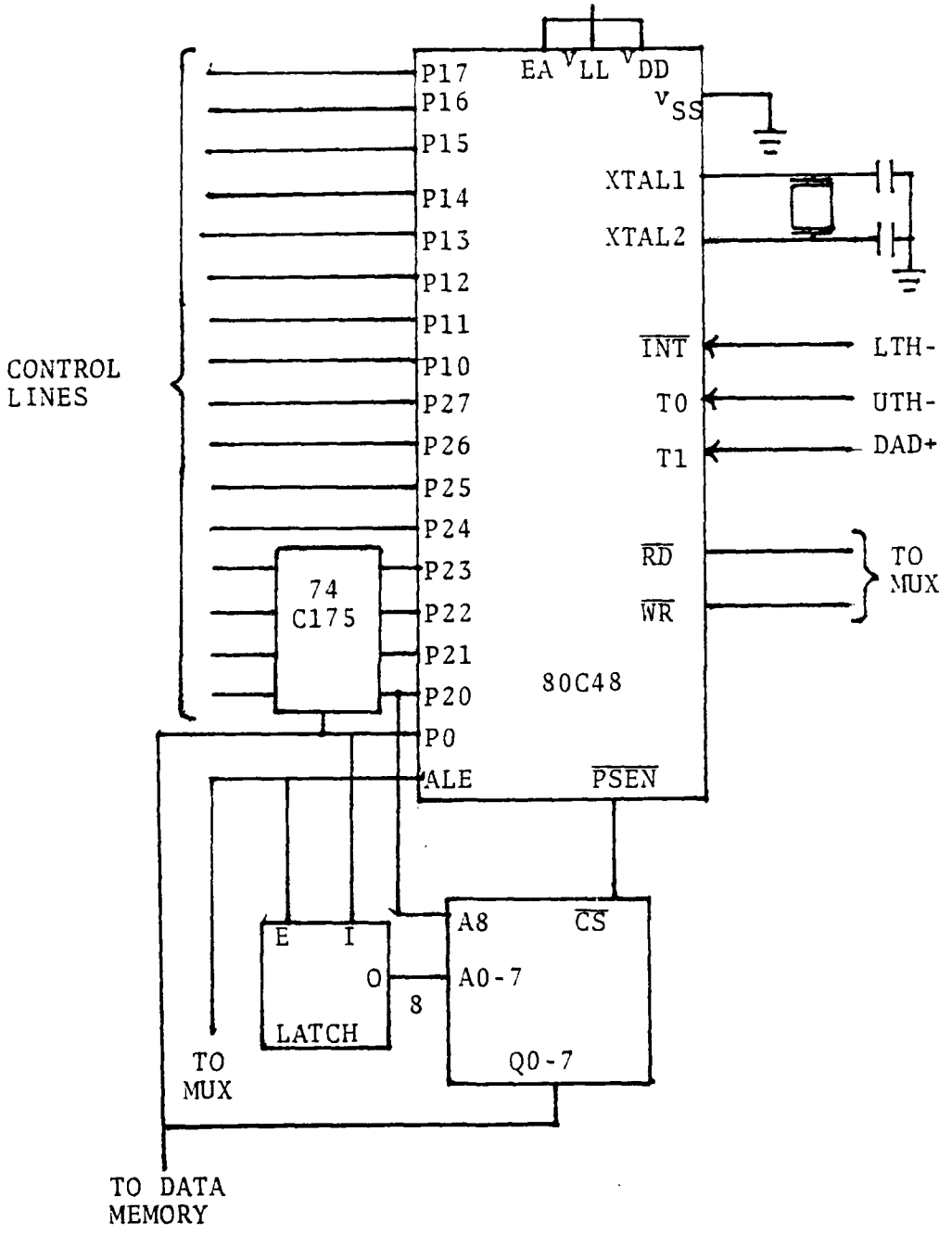


Fig. 12. CPU2 Acquisition Circuit

media is three 74C173 Quad Tri-State D Flip-Flops, as shown in Fig. 13. To write, P21 goes low, disabling the control lines and allowing data to be written to the 74C173's. To read, P22 goes low, disabling the control lines and allowing the data to be read from the three 74C173's. The power is never shut off to these devices.

7. The Shift Registers

The conversion of the parallel data from the intermediate data memories to the serial data for the data recorder is accomplished by three 74C95 4-bit Shift Registers. The time base for the shift is derived from the ALE signal with its pulse extended by a 74LS122 fed into an ICL 8240. A shift is executed on each high to low transition of the output of the 8240. The circuit is shown in Fig. 14.

Parallel load is accomplished by the read signal triggering the output of a CMOS 555 Timer to go from low to high. This signal is fed to the mode control line of the shift register. On the next high to low transition of the 8240 output, the new data is clocked into the shift register.

8. The MFM Encoder

The MFM encoder is a combinational logic circuit that takes the serial output of the shift register and converts it to the MFM code, See Fig. 2. In the acquisition circuit, the encoder is the interface between CPU2 and the data recorder. Synchronization is based on two instruction cycles per bit period.

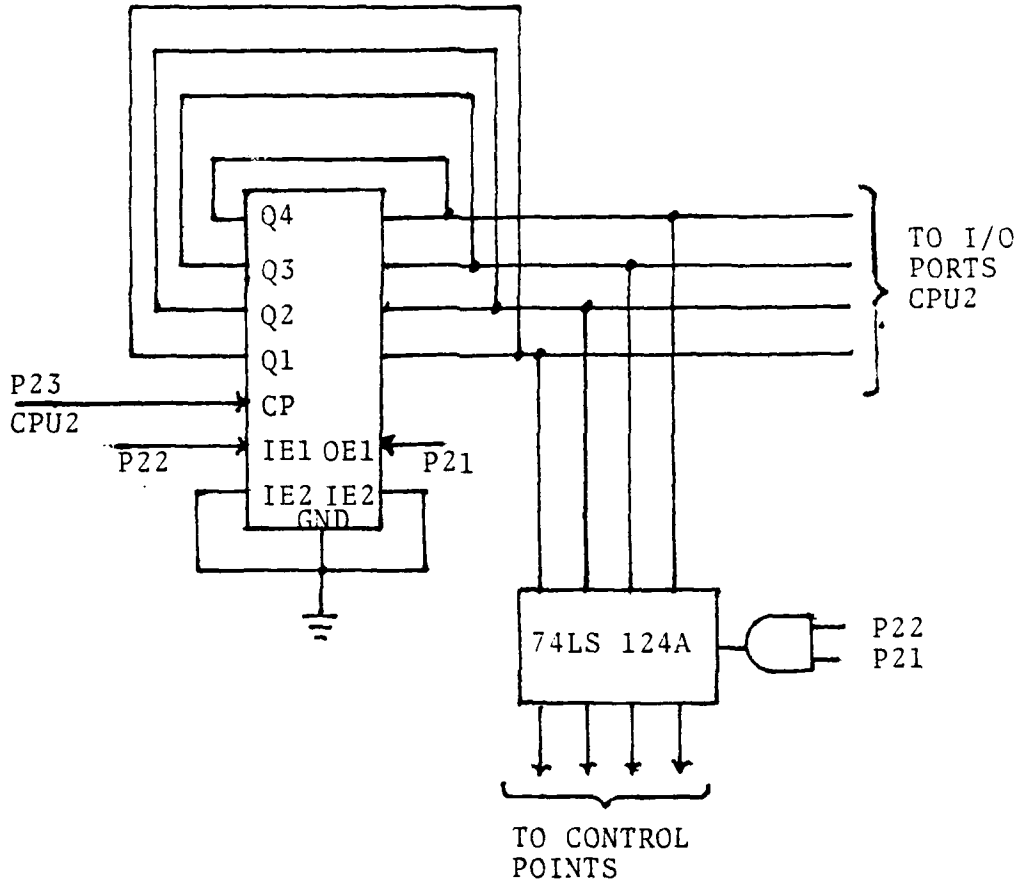


Fig. 13. Track and Block Count Storage One of Three 74C173

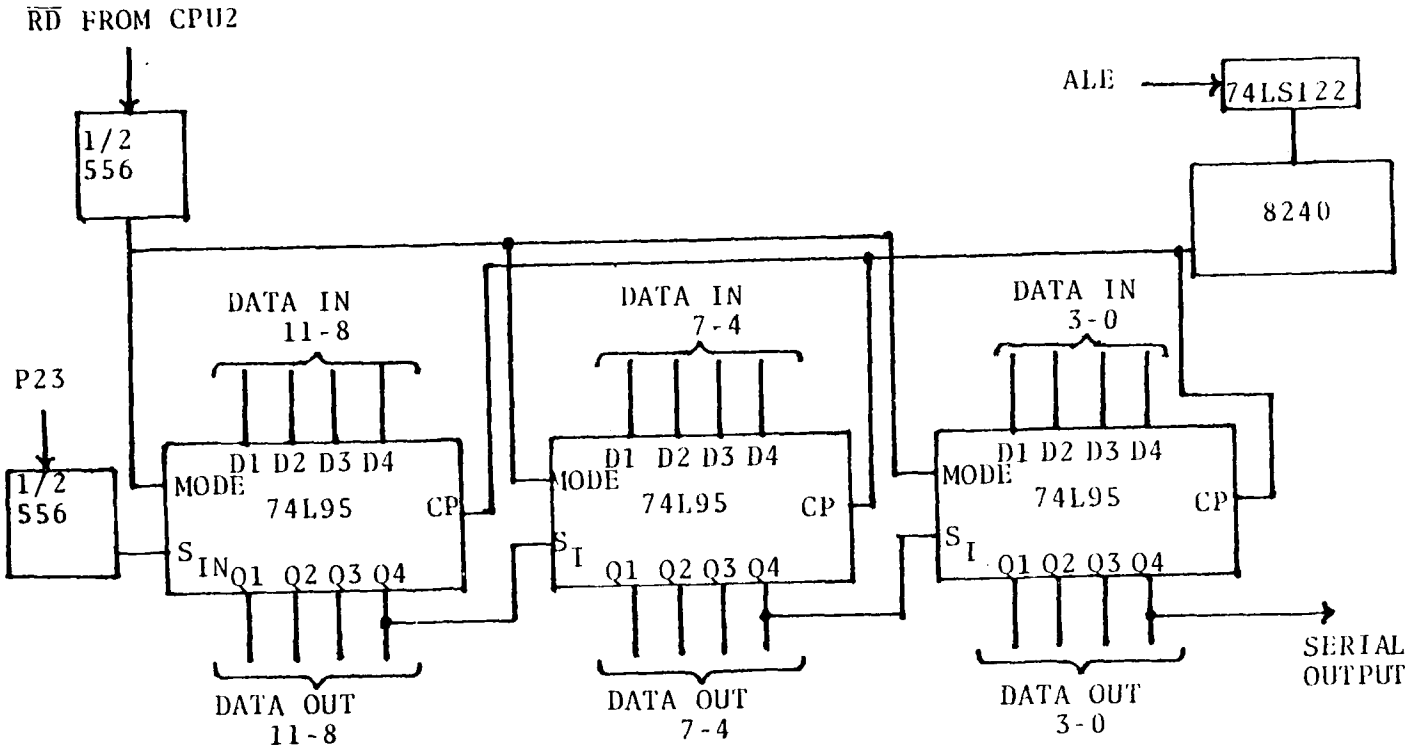


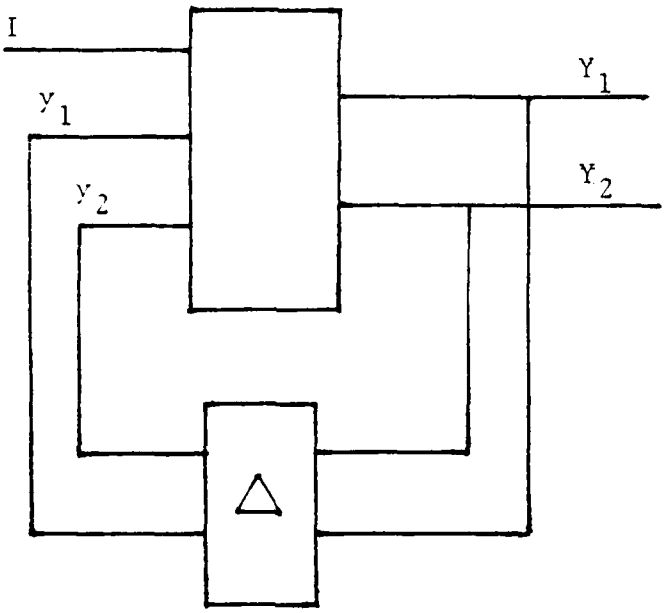
Fig. 14. Shift Register

The code is generated by taking the serial output of the shift register in combination with the two previous half bit period levels fed back to the input of the encoder, see Fig. 15. The truth table shows the inputs y_1, y_2 and I determining the outputs Y_1 and Y_2. The input y_1 and y_2 are the two previous half bit period levels. The input I is the current data input. The outputs Y_1 and Y_2, to be output sequentially, are the two encoded half bit period levels of the current data bit. The sequence on the inputs from 000 to 111 lends itself to a straightforward implementation using two eight input multiplexers and flip-flops as feedback.

The timing is derived from the ALE signal and the output of the 8240 timing the shift register.

The encoder is constructed of two 74C151 Eight Input Multiplexers and three 74C74 Dual D Flip-Flops. The inputs of the two multiplexers are tied to the levels dictated by the truth table for Y_1 and Y_2. The selects are the inputs y_1, y_2, and I. The multiplexers are enabled sequentially with the outputs clocked into the first of the two 74C74's for feedback. The second 74C74 clocks these two levels to the select lines of the multiplexers at the same time the data arrives. The circuit is shown in Fig. 16.

The initial state is the first entry in the truth table. The multiplexers will output 1 1 when enabled by the E_1 and E_2 signals. The sequential enabling of the multiplexers



a. THE MFM ENCODER

y_2	y_1	I	Y_1	Y_2
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	0

b. THE TRUTH TABLE

Fig. 15. The MFM Encoder

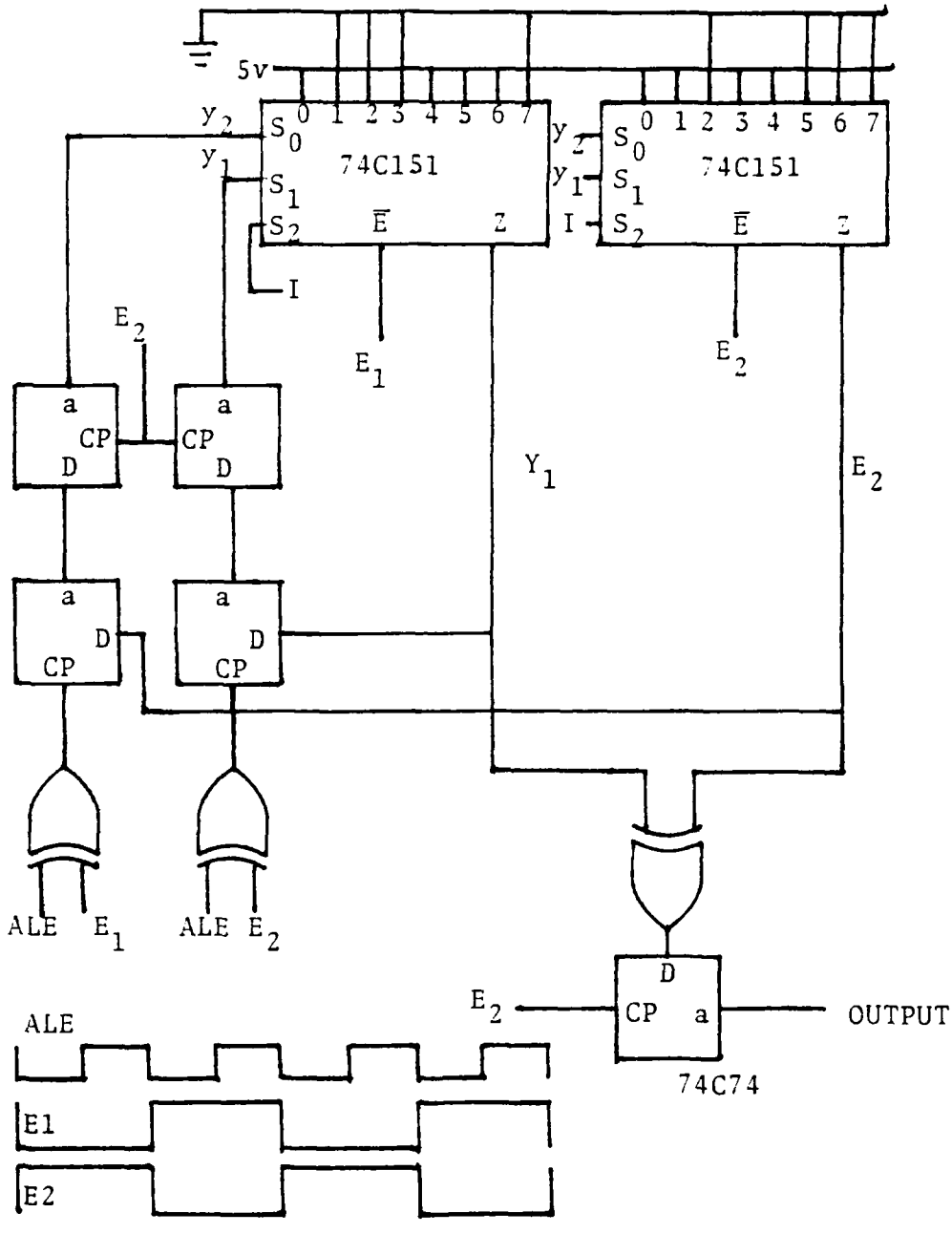


Fig. 16. The MFM Encoder Circuit

outputs the level which is clocked into the output 74C74 at the same time it is clocked into the feedback path. The output then continues according to the truth table.

The feedback path requires two stages. One stage for the intermediate levels and one stage for the selects to the multiplexers. The first stage is clocked into one 74C74 at the mid point of the enabled multiplexers output. The first half bit period level is stored at the low to high transition of the logical exclusive OR of E_1 and ALE. The second half bit period level is clocked in at the low to high transition of the logical exclusive OR of E_2 and ALE. The two previous half bit period levels are clocked through to the selects of the multiplexers at the same time with the low to high transition of E_2.

9. The Data Recorder

The input signals for the data recorder are provided by CPU2. The device select (SL1-) is an active low signal enabling the recorder to respond to input signals. The write enable (WEN-) enables the write and erase functions. This signal should be set prior to starting the tape and left on after the tape has been stopped and the recorder deselected. The data write signals (WDA-,WDA+) are offered in both active low and active high. This signal is received from the LM 360 Comparitor at the output of MFM encoder. Forward and reverse (FDW-,REF-) are both active low. When both are false at the same time, the tape motion

is stopped. If both are set true at the same time, no damage will be done to the drive; but the direction of motion is uncertain. The high speed (HSP-) signal causes tape motion at 90 inches per second in the direction dictated by FDW- and REV-. The signal is used during the rewind at the end of each track. The track select signals (TR2-, TR1-) select the track to be read or written to.

The output signals from the data recorder are provided to CPU2. The upper tape hole signal (UTH-) and the lower tape hole signal (LTH-) are provided to TO and $\overline{\text{INT}}$, respectively. LTH- is of particular significance since the only place the lower tape hole appears is toward one of the physical ends of the tape. The assertion of LTH- causes a vector to the interrupt service routine in CPU2. The upper tape hole marks the beginning of the tape, the load point and the early warning hole. All tape holes are in accordance with ANSI standard X3.55-1977, Fig. 3. The data read (RDA-, RDA+) are offered in both active high and active low. The choice of active high or low in the read should agree with that of the data write to avoid data inversion. Data detect (DAD+,DAD-) indicates data is present on the tape during a read or search.

B. THE RECONSTRUCTION CIRCUIT

The data acquisition circuit just described was designed to function under severe power constraints. The reconstruction

circuit is not subject to this constraint since it will be operating in a laboratory environment. This means the CMOS circuits used before can be substituted with TTL or MOS circuits. The long sampling period can be condensed to cut the time required to reconstruct the data with scaling transforming the spectrum of the data back to its original place. The A/D will be changed to a digital-to-analog converter (D/A). The leads for the input and output for the intermediate data memory must be interchanged since CPU1 is now reading from the memory and CPU2 is writing to the memory. Finally CPU1 and CPU2 need not be the CMOS 8048 but the MOS 8748 with on chip program memory. The use of the 8748 will significantly ease the timing. There are many similarities between the acquisition and the reconstruction circuits; only the changes will be discussed.

1. Central Processing Unit One

There is no non-sampling interval timer, or sampling period timer. The number of blocks to be included in each sampling interval is still needed to separate sampling intervals or reduce the duration of data examined at one time. The resulting circuit is shown in Fig. 17.

2. Central Processing Unit Two

The only change in CPU2 is the elimination of the external registers to store the block count and track. The block count and track will be stored internally. The circuit is shown in Fig. 18.

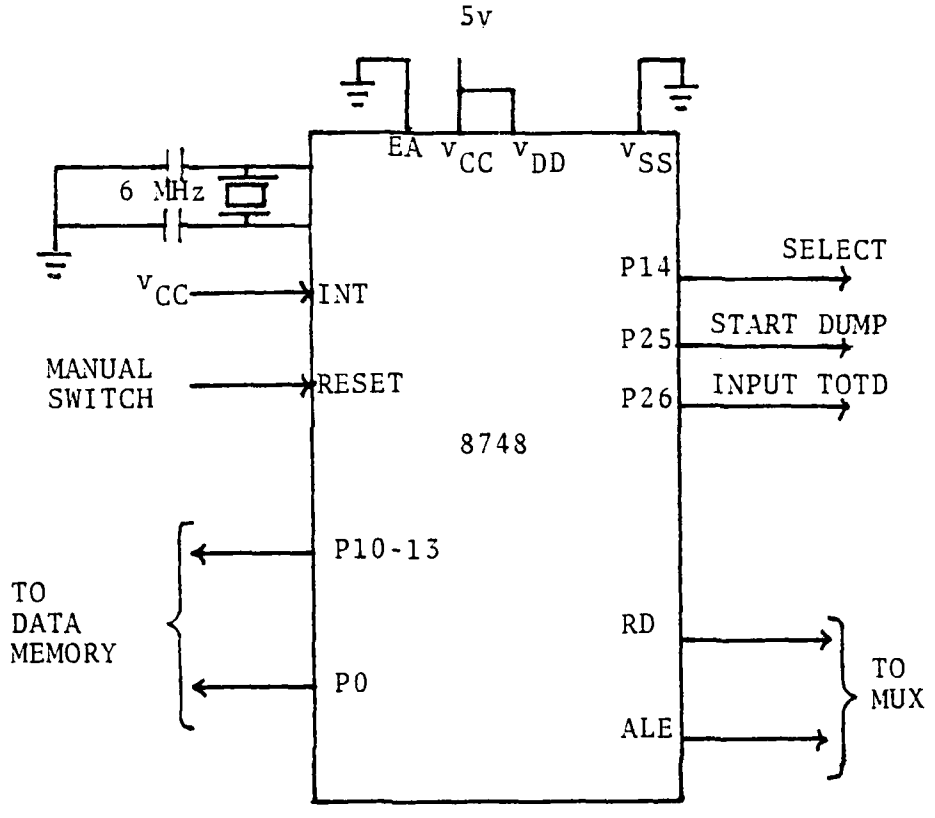


Fig. 17. CPU1 For Reconstruction Circuit

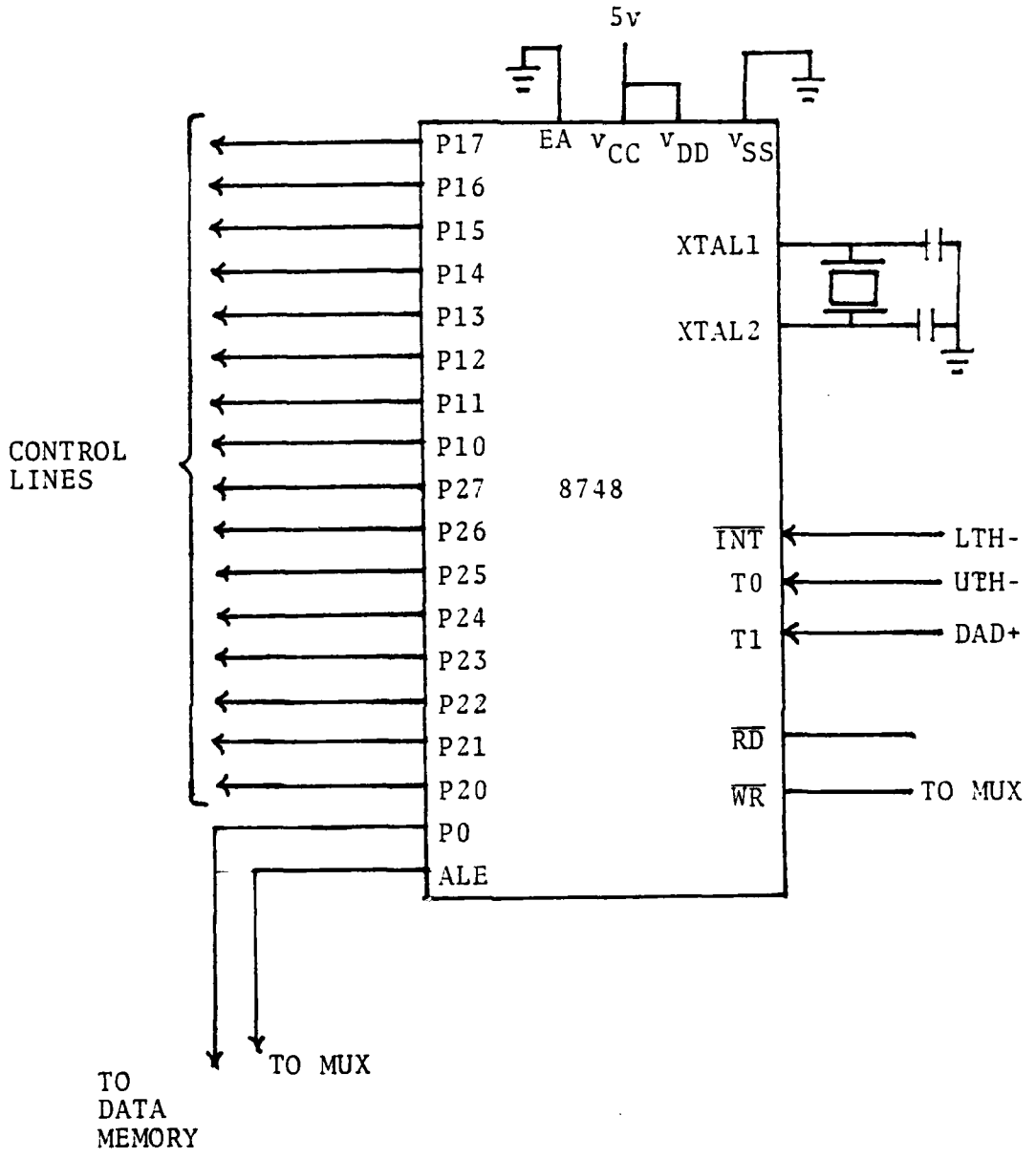


Fig. 18. CPU2 For Reconstruction Circuit

3. The Digital to Analog Converter

The digital to analog converter (D/A) used in this design is the Intersil ICL 7112 12 Bit Multiplying D/A Converter [3]. The device and circuit is shown in Fig. 19. The device is connected in a unipolar or bipolar mode.

4. The MFM Decoder

The MFM decoder takes the output from the data recorder and converts it to the "1's" and "0's" of the data. This circuit is the interface between the data recorder and CPU2. The decoder looks at the two half bit period levels from the recorder. If the two half bit period levels of the tape output are the same, both high or both low, the data bit is a "0". If the two half bit period levels are different, the data bit is a "1". The differentiation between the data "1" and the data "0" is accomplished by a logical exclusive OR of the two half bit period levels.

The difficulty is the synchronization of the tape output, the decoder, the shift register, and CPU2. The requirement is that the tape output be synchronized with the decoder which must provide a correct and stable data value for two instruction cycles. This is required to clock the output of the decoder into the serial input of the shift register. The shift register is synchronized with CPU2. To achieve this synchronization, the decoder must have a time base that is triggered by the output of the data recorder and must be independent of the time base of the shift

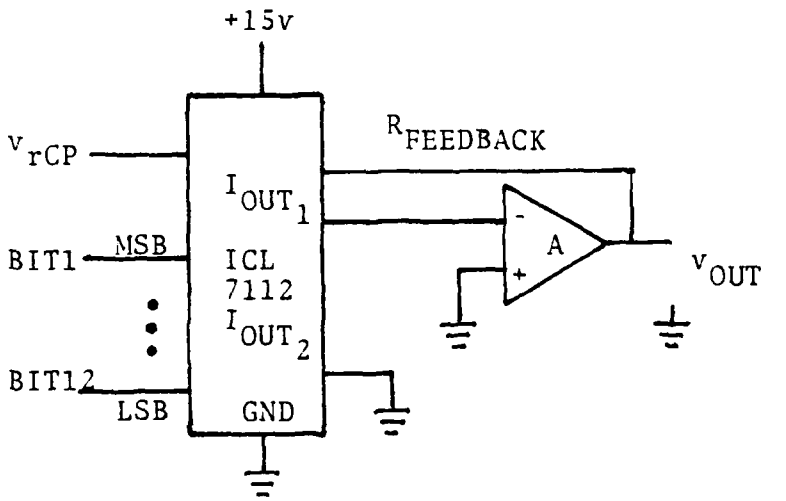


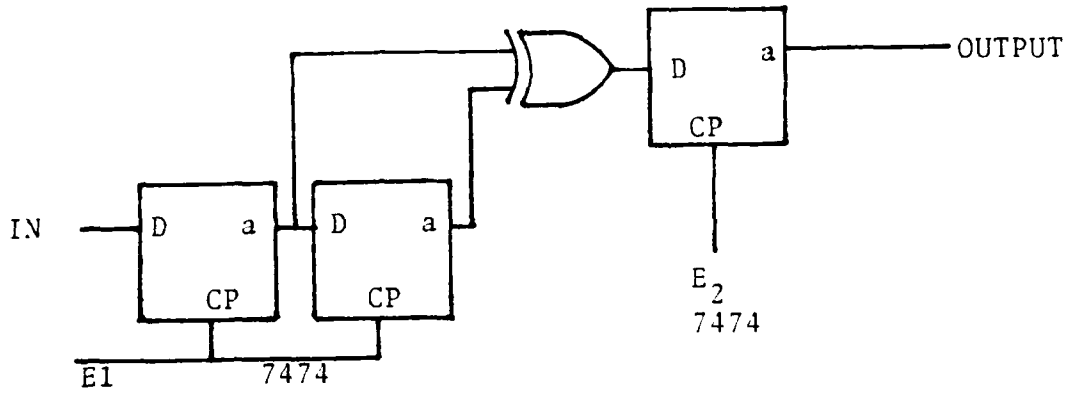
Fig. 19. Digital-To-Analog Converter [3]

register and CPU2. The independence is necessary because the data may not appear synchronized precisely with the time base of CPU2.

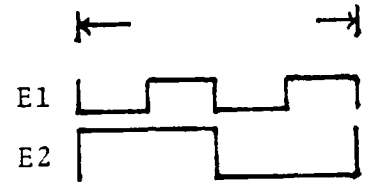
The decoder circuit consists of two 7474 Dual D Flip- Flops and an exclusive OR gate, as shown in Fig. 20. The time base is a square wave of a period one half that of the bit period and a square wave of a period of the bit period. The bit period is 5.25 micro seconds, the same used in the encoder. The faster of the two signals, E_1, clocks the first of the two 7474's. This pair acts as a shift register. After two consecutive low to high transitions, the two half bit period levels are exclusively ORed', and the result is clocked into the first flip-flop of the second 7474 by E_2. This value will be stable for the required two instruction cycles.

The time base for the decoder is established by an ICL 8240 shown in Fig. 20. The period is determined by the values of the resistor and capacitor.

The data is received from the 75110 Line Driver connected to the data read of the data recorder. This output will be used to trigger the 8240 as well as input the tape signal to the decoder. The string of "0's" in the preamble of the data block will either start high and go low or vise versa. The trigger to the 8240 will occur on the first low to high transition. The first half bit period level will be



a. THE CIRCUIT



b. THE TIMING SIGNALS

Fig. 20. The MFM Decoder

clocked into the first flip-flop at the midpoint of the first half bit period. The second half bit period level will be clocked in at the mid point of the second half bit period. The clock signal is E_1. With the two half bit period levels present in the two flip-flops, the result of the exclusive OR is clocked into the second 7474 by the low to high transition of E_2.

When the preamble "1" is encountered, the low to high transition at the output of the decoder triggers the 8240 controling the shift register. This trigger inputs the decoded level to the serial input of the shift register. The subsequent data is clocked into the shift register on each high to low transition. This scheme insures the synchronization of the shift register with the decoder. With data clocked into the shift register, CPU2 can now write the data to the intermediate memory every 24 instruction cycles.

C. POWER SWITCHING

Power is provided to the various parts of the acquisition circuit only during those times when that part is performing a function. The power structure is broken into three sections: always on, on with CPU1 and on with CPU2. The always on components are the non-sampling interval timer, the track and block count storage registers, and the power switching network. On with CPU1 is its peripheral elements and the intermediate data memories. On with CPU2 is its

peripheral elements, the MFM encoder and the data recorder. No power is provided to CPU1 or CPU2 during the non-sampling interval.

No specific power supply circuits have been identified for use in this design, though several have been tested. When the power signal is true, the power supply will offer power at the prescribed voltage and current.

The power switching timing diagram is shown in Fig. 21. The first action occurs when the non-sampling interval timer output goes from low to high at the end of the non-sampling interval. This triggers power and a reset pulse to CPU1. When P25 of CPU1 goes low CPU2 is reset for a dump. This action brings power up to CPU2 and the data recorder, and provides a reset signal to CPU2. When the shut down signal of CPU2 goes low, power is cut to CPU2 and the data recorder.

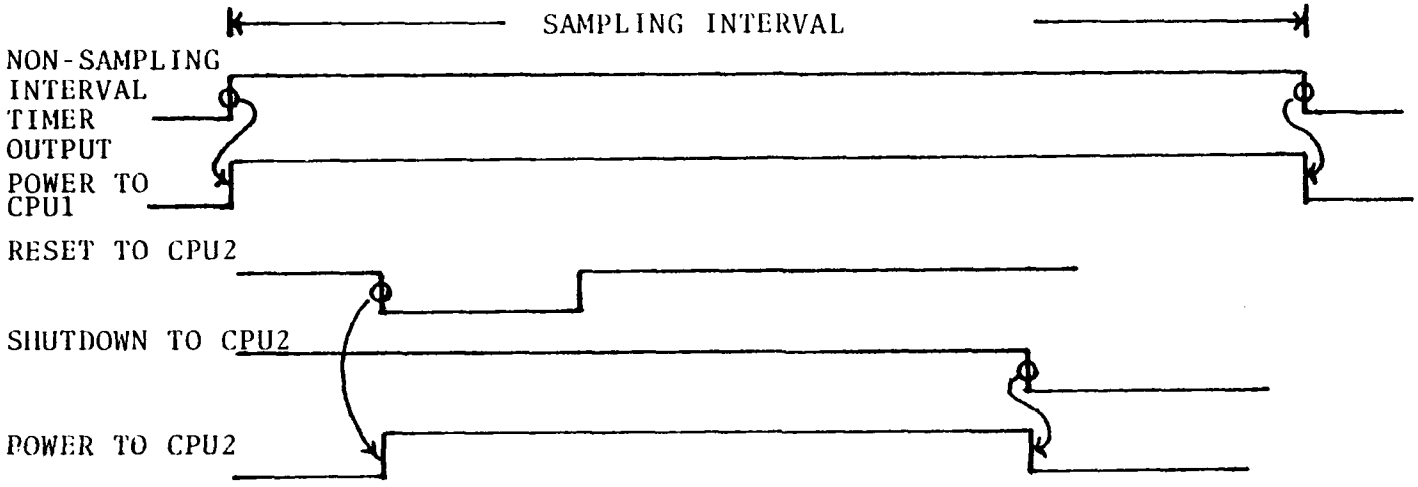


Fig. 21. Power Switching Timing Diagram

V. SOFTWARE

The software consists of four routines. Each routine will be explained individually with its flow diagram. The complete programs are shown in Appendix B. The four routines are the data acquisition routine, the write to tape routine, the data reconstruction routine, and the read from tape routine.

A. THE DATA ACQUISITION ROUTINE

The data acquisition routine directs CPU1 to take a sample on a regular basis, convert that sample to a digital representation, and store the data word in intermediate memory. The flow diagram is shown in Fig. 22.

The routine starts with the input of the number of blocks to be taken during the sampling interval. The variable is named TOTD. The select signal is the least significant bit of TOTD, which alternates between "0" and "1" as TOTD is decremented. If TOTD is zero, the sampling is to be continuous, no non-sampling interval. The page and address are initialized. The first address is 111111111111, FFF hexidecimal, and the last address 000 hex. The select and page number is output to the memory. A wait state is entered for the sampling period to be completed. At the end of the sampling period the counter overflows from 255 to 0

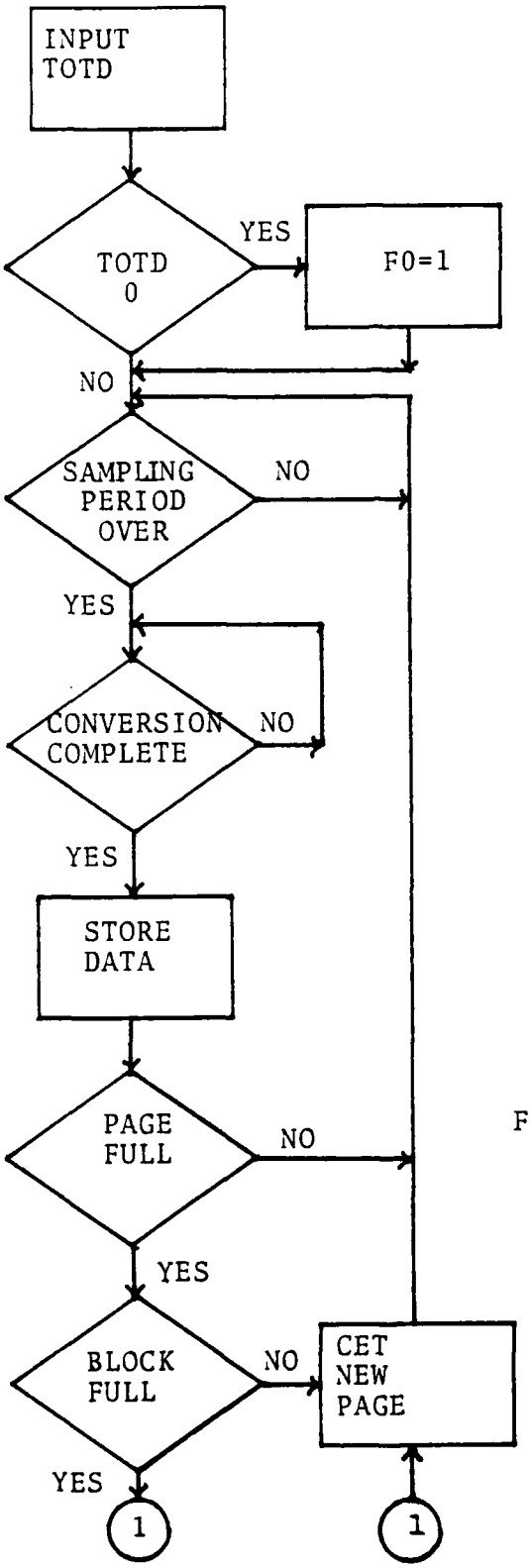


Fig. 22. Data Acquisition Routine Flow Diagram

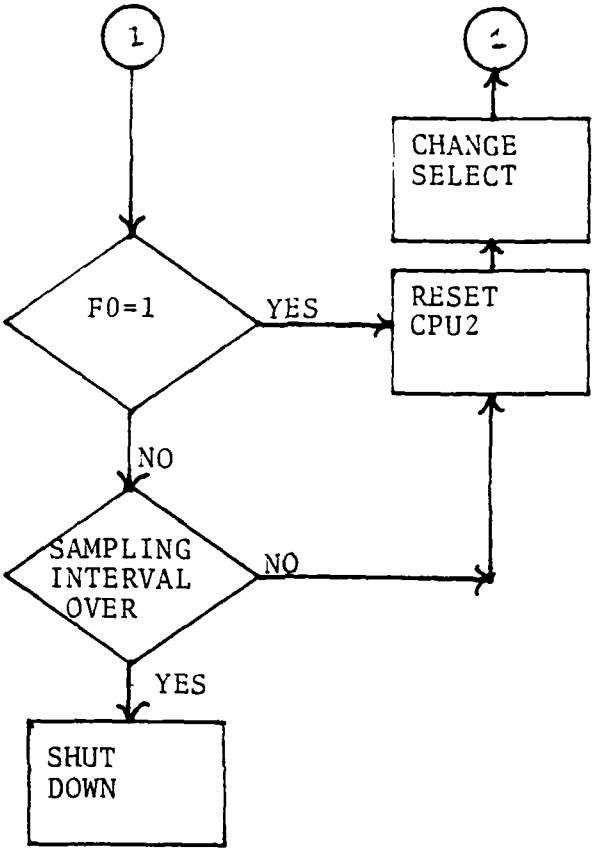

1
2
CHANGE
SELECT
F0=1
YES
RESET
CPU2
NO
SAMPLING
INTERVAL
OVER
NO
YES
SHUT
DOWN

Fig. 22. con't.

and interrupts to the counter interrupt service routine signaling for a start conversion. The wait state is reentered for the conversion to be completed. When the conversion is completed the external interrupt is asserted, and the interrupt service routine stores the data. The number of samples taken on that page is tested, and if not yet 256, the routine returns to the wait state for the end of the next sampling period. If the page is full the routine checks for a full block, 16 pages. If the block is not full, the page number is advanced with the same select; and the wait state is entered for the next sampling period. If the block is full, the select is changed by decrementing TOTD; and CPU2 is reset to dump the block just filled to the data recorder. The first page of the new block is established, and the wait state is entered for the next sampling period. If TOTD is decremented to zero, the flag is tested. If the flag is not set, a wait state is entered for CPU2 to complete the dump on the last block, then the non-sampling interval timer is triggered shutting down CPU1 and the intermediate memories. If TOTD was originally zero, the flag is set; and the routine continues to obtain data as in the previous block changes.

B. THE WRITE TO TAPE ROUTINE

The write to tape routine controls CPU2. It directs data to be taken from the intermediate memories and written to the data recorder. The routine has three parts: the

initialization, the write to the data recorder, and the shut down. The flow diagram is shown in Fig. 23.

When the system is first powered up before being placed on the ocean floor, the registers storing the track and block count are cleared to zero. This flags the first write. The routine starts with the input of the track and block count after being reset by CPU1. If this is zero, track one is selected; and the block count is initialized to 606. The tape which has been preset to its physical beginning, is advanced to 4.8 inches beyond the load point hole, see Fig. 3. If the input is not zero, the current track is set; and the tape is run in the reverse direction until data detect becomes true. This point is the end of the previous block. The tape is then stopped. The direction is set for forward and started again. When the data detect goes false, the tape is stopped. From this position the tape is prepared for the block of data to be written. This reverse run insures the tape is positioned immediately after the previous block and is properly tensioned to improve recording performance.

The writing to the data recorder begins with write enable being set true. The tape is started in the forward direction and the 1.2 inch inter-block gap is passed. At the end of the interblock gap, the 39 "0's" and the "1" of the preamble are written to the tape. Twenty-two instruction cycles after the "1" is input to the shift register, the

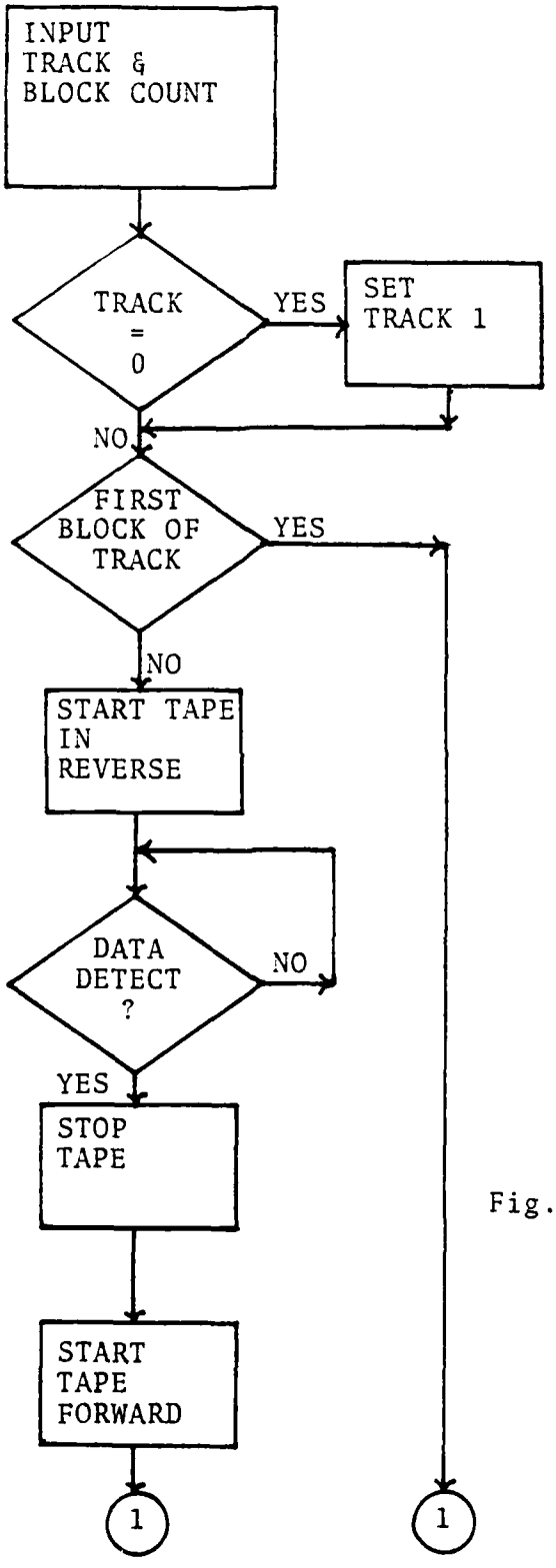


Fig. 23. Write To Tape Routine Flow Diagram

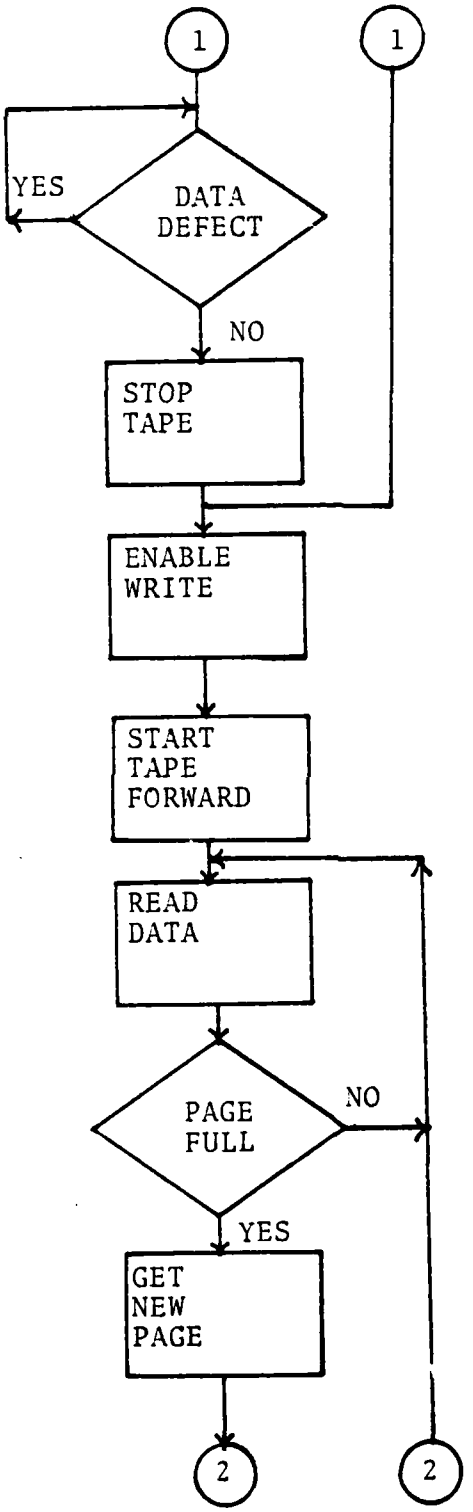

1
1
YES
DATA
DEFECT
NO
STOP
TAPE
ENABLE
WRITE
START
TAPE
FORWARD
READ
DATA
PAGE
FULL
NO
YES
GET
NEW
PAGE
2
2

Fig. 23, con't.

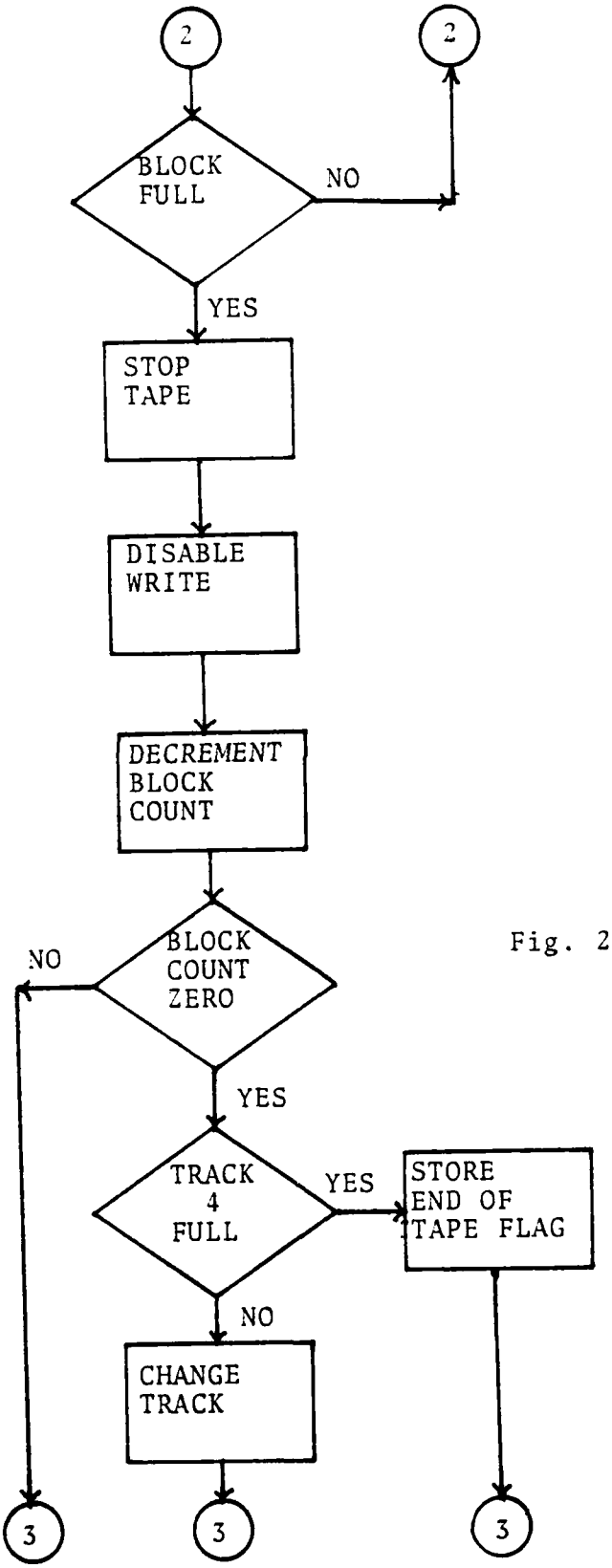

2
2
BLOCK FULL
NO
YES
STOP TAPE
DISABLE WRITE
DECREMENT BLOCK COUNT
BLOCK COUNT ZERO
NO
YES
TRACK 4 FULL
YES
STORE END OF TAPE FLAG
NO
CHANGE TRACK
3
3
3

Fig. 23. con't.

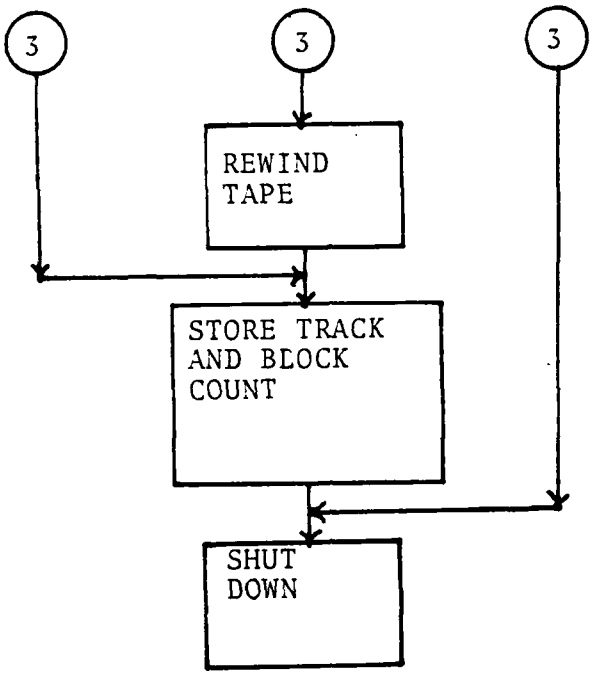


Fig. 23. con't.

first data word from the intermediate data memory is written to the shift register, with another data word written each 24 instruction cycles thereafter. When the last word has been written to the tape, the string of 39 "0's" are written and the tape stopped. The data recorder is deselected and the write enable is set false.

The shut down section decrements the block count and tests for zero. If it is not zero, the new block count and the present track are stored, and CPU2 and the data recorder are shut down. If the block count is zero, the track is advanced; and 606 is written to the external storage. The data recorder and CPU2 are then shut down. If this is the last block recorded on track four, the data recorder is full. To flag this condition all "1's" are written to the track and block count registers.

C. THE DATA RECONSTRUCTION ROUTINE

The data reconstruction routine controls CPU1 in the reconstruction of the data collected. The routine commands CPU2 to fi-l alternating blocks of intermediate memory and sequences CPU1 through this data providing it to the D/A. The flow diagram is shown in Fig. 24.

The routine begins by inputting the number of blocks per sampling interval (TOTD). Again, if TOTD is originally zero the data is taken continuously. A select is output, and CPU2 is reset to fill that block of intermediate memory.

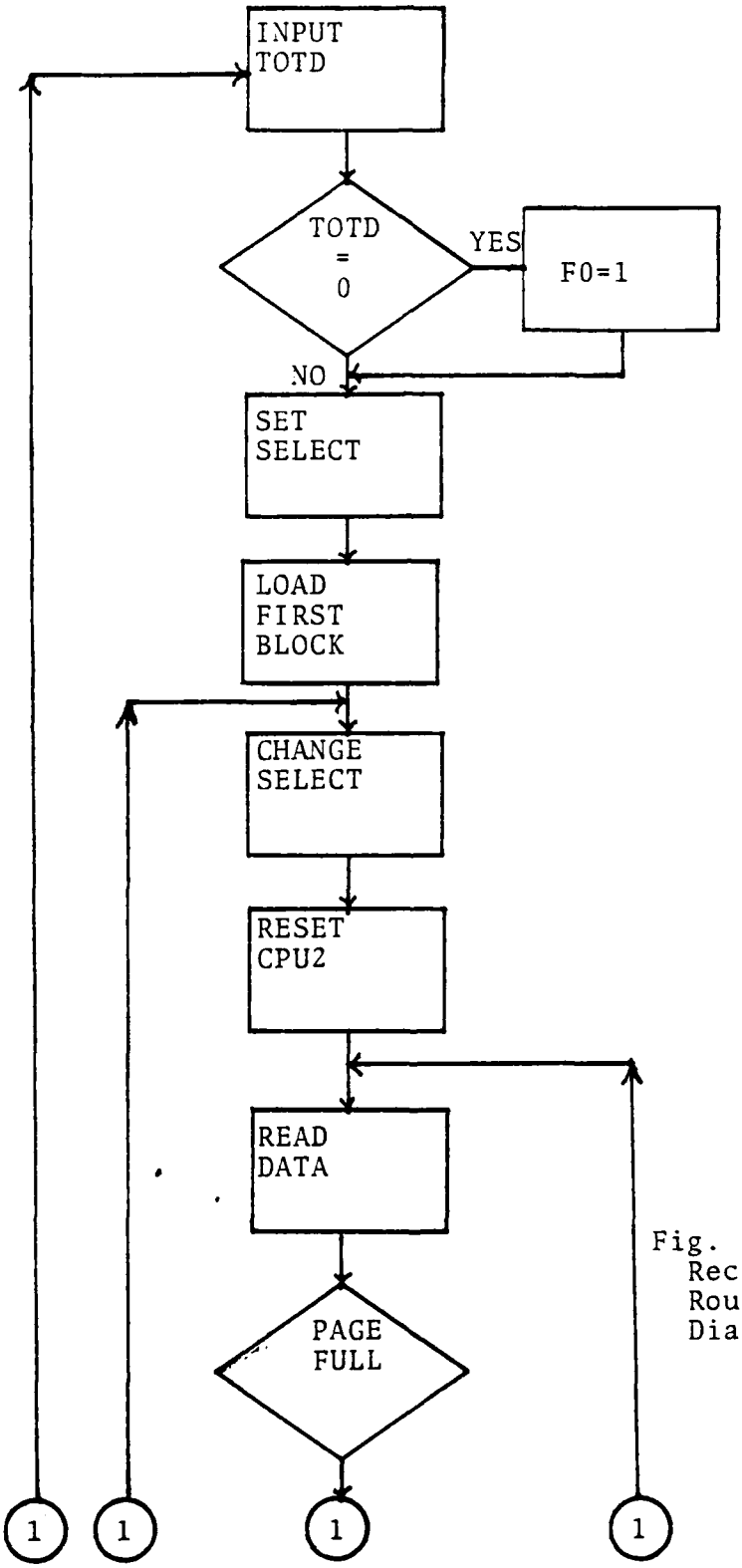


Fig. 24. Data Reconstruction Routine Flow Diagram

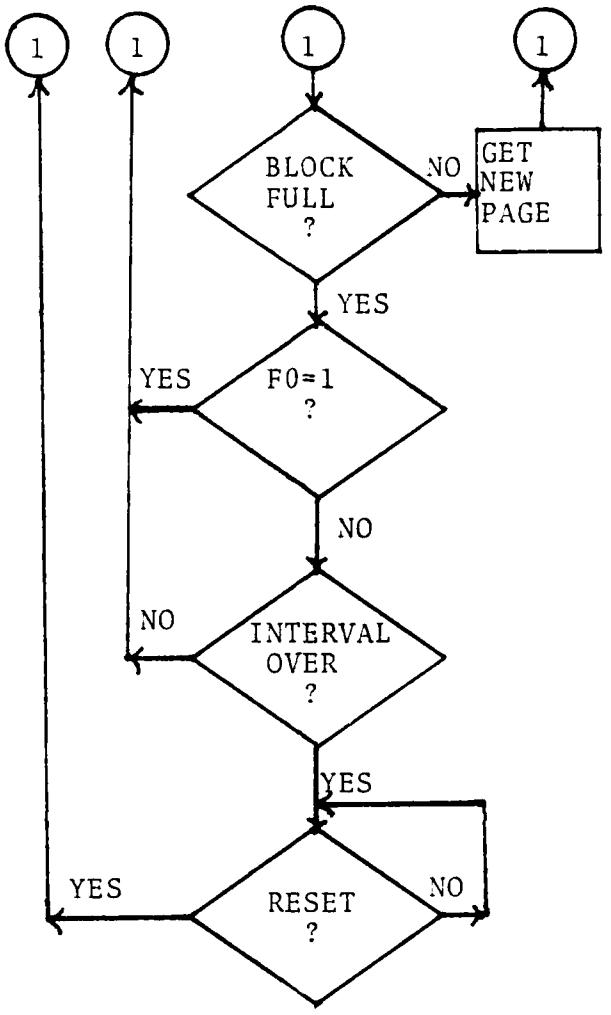

1
1
1
1
BLOCK FULL ?
NO
GET NEW PAGE
YES
YES
F0=1 ?
NO
NO
INTERVAL OVER ?
YES
YES
RESET ?
NO

Fig. 24. con't.

When the block has been filled, select is changed, CPU1 begins the reconstruction of the data, and CPU2 is reset to fill the alternate block of intermediate memory. CPU2 is reset each time CPU1 changes select. This sequence allows a continuous flow of data to the D/A. The data can be reconstructed as fast as 8000 times the original data acquisition rate.

TOTD is decremented and tested at the end of each block. If found to be zero, CPU1 activates an audible or visual signal to indicate the sampling interval has elapsed and enters a loop waiting for a manual reset to start the routine from the beginning. If TOTD was originally zero the reconstruction operation continues without activating the signal. This manual reset allows the operator an opportunity to make any adjustments necessary.

D. THE READ FROM TAPE ROUTINE

The read from tape routine controls CPU2 and the data recorder. The routine causes the tape to be read and the data written to the intermediate memory. As with the write to tape routine, the program is broken into three blocks: the track initialization, the read from tape, and the shut down. The flow diagram is shown in Fig. 25. All three parts are very similar to the corresponding parts of the write to tape routine. Only the differences will be discussed.

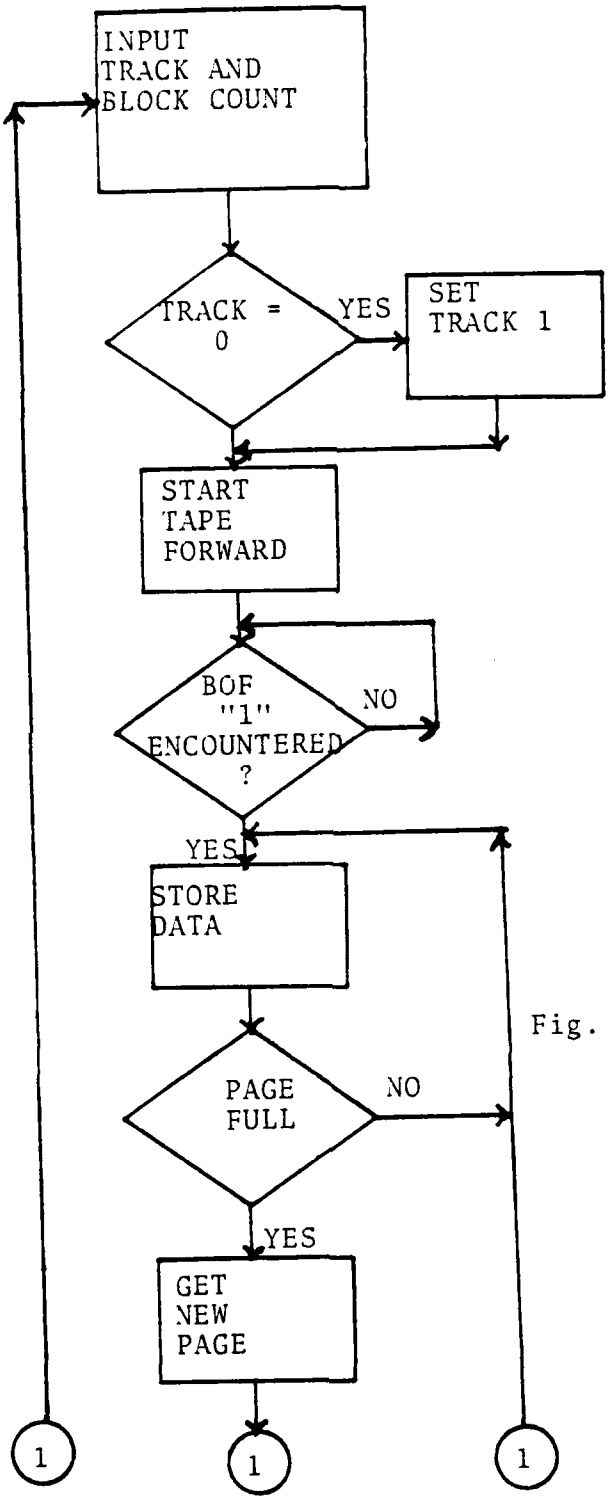


Fig. 25. Read From Tape Routine Flow Diagram

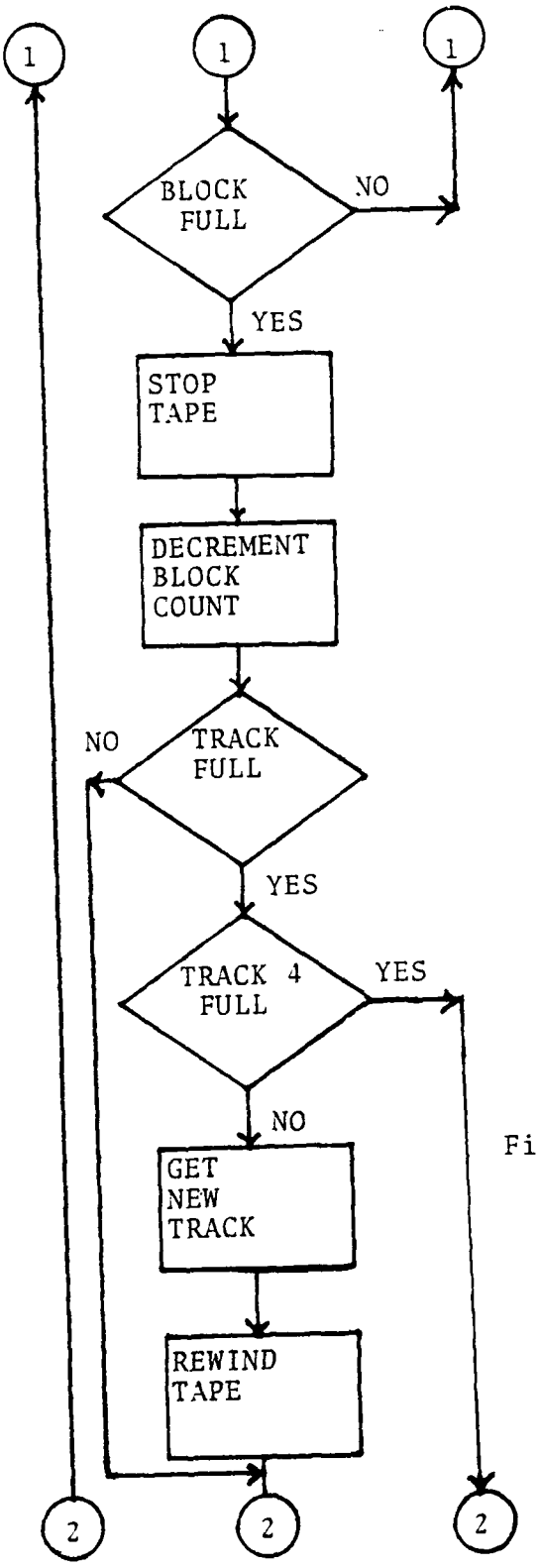

1
1
1
BLOCK FULL
NO
YES
STOP TAPE
DECREMENT BLOCK COUNT
NO
TRACK FULL
YES
TRACK 4 FULL
YES
NO
GET NEW TRACK
REWIND TAPE
2
2
2

Fig. 25. con't.

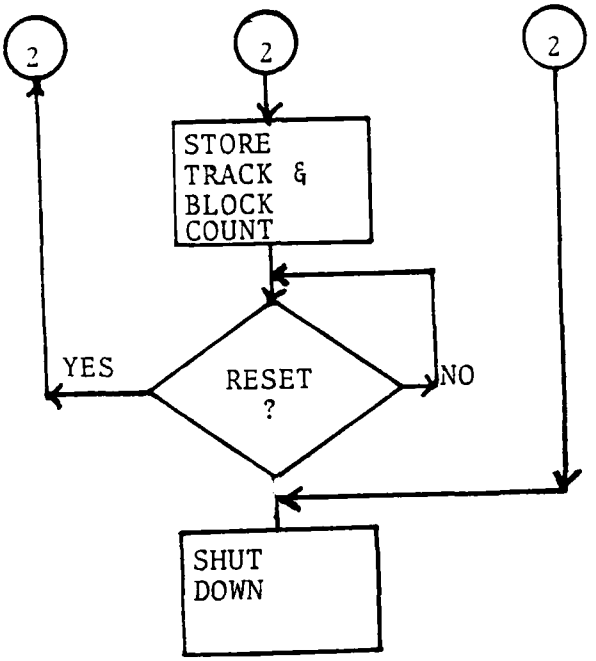


Fig. 25. con't.

The only change in the track initialization routine is there is no need for the reverse run since the power is never removed from the data recorder.

When the track has been initialized at the beginning of the track or between two blocks, the tape is started in the forward direction. The preamble synchronizes the MFM decoder and the one of the preamble starts the shift register. When the one is shifted into the fifth bit of the shift register, the program and the shift register are synchronized. Thirteen instruction cycles later the first data word of the block is written to the intermediate data memory. Every 24 instruction cycles thereafter, the next data word is written to the data memory, filling the remaining 4095 locations.

At the end of the read cycle the data recorder is stopped. The track and block count are tested and the track changed if necessary and stored in the internal registers. The routine enters a loop waiting for TO to go low, as directed by CPU1, to read the next block.

VI. TEST AND EVALUATION

All software intended for the final verion of the design was programmed into an INTEL Prompt 48 development system. Input and output control signals were tested. Output signals were connected to light emitting diodes (LED's). All four routines were tested and debugged. All performed as intended.

The test circuit was restricted to an eight bit version of the data acquisition circuit without a data recorder. Control signals intended for the data recorder were demonstrated by turning on and off LED's. The intermediate data memories were made up of two 1 K by four bit static RAM circuits. This restricted the intermediate memory to four pages. The input data was an arbitrary bit pattern input directly to each intermediate data memory individually. The two bit patterns were made different to distinguish between the two memories and to demonstrate the memories were being alternated between read and write cycles. The circuit was connected on two boards from TTL and MOS components. The two processors were two INTEL Prompt 48 development systems. The software was only modified to conform to the eight bit data and the requirements of the Prompt 48's.

The data acquisition system was stored in the Prompt 48 designated CPU1. The event counter was triggered by an

external square wave input. To demonstrate that the data was written to the intermediate memories and could be read and converted to a serial bit stream, the Prompt 48 designated CPU2 was programmed to continuously read the memory that was available to it.

The output of this test circuit demonstrated that the two memories were being alternated as intended. The data was input and written to the proper memory by CPU1. CPU2 was triggered and read the available memory. The data read from the memory, was input to the shift register and output serially. The serial output was fed into the MFM encoder and properly encoded.

VII. FINAL TEST PROPOSAL

The complete design can be constructed and tested when the DEI data recorder described in this thesis is available. With the data recorder, the system should be implemented with the components described in this thesis. The data obtained previously from the current analog system can be used as the input data to the digital system. The spectrum obtained from the output digital system can then be compared with the spectrum obtained from the analog system. This comparison can be used to determine if the digital system is performing as intended.

VIII. CONCLUSION

The purpose of this thesis was to develop a digital data acquisition system for use in the study of the earth's magnetic field. The device described in this thesis could perform this function on the ocean floor; and, with minor modification to the hardware and software, the system could be connected to a radio transmitter for use at remote land sites instead of being connected to the data recorder. Two areas require additional attention.

First, the power supplies and power switching system are the most important areas requiring attention. The final development of the power system described in Section IV.C. has not been realized. This system is needed for the final implementation of the acquisition system.

Second, the temperature test of the DEI 3400 Funnel data recorder will be required prior to final implementation of the design. If the data recorder is not able to withstand the temperature extremes encountered on the ocean floor, the data recorder control hardware and software must be modified to accommodate a different data recorder.

The data acquisition system described in this thesis is a viable alternative to the current analog acquisition system used in the geomagnetic field study to date. Alternative CMOS microprocessors are available, however, the CMOS

version of the INTEL 8048 single chip microcomputer appears to provide the best means of implementing the concept due to its capabilities. Further development of this system is recommended.

APPENDIX A

Extracted from Product Specification Series: CMTD-3400 S2
Drive 6400 BPI

Specification Summary

Details for each item below can be found in the body of this specification.

PARAMETER		VALUE
I.	DATA:	
	TRANSFER RATE	192×10^3 BITS/SEC
	CAPACITY, UNFORMATTED	17.3×10^6 BYTES
	CAPACITY, FORMATTED (8K BYTE BLOCK)	15.2×10^6 BYTES
	RECORDING FORM	HEAD UP FROM BOT (ANSI)
	RECORDING CODE	MFM
	HEAD FORMAT	READ WHILE WRITE WITH ERASE
	NUMBER OF RECORDED TRACKS	FOUR
	RECORDING DENSITY	6400 BITS/IN
	DATA RELIABILITY	
	SOFT ERROR RATE	$\leq$ 1 ERROR IN 10^8 BITS
	HARD ERROR RATE	$\leq$ 1 ERROR IN 10^{10} BITS
II.	MOTION:	
	SPEED, READ WRITE	30 IN/SEC
	SPEED, SEARCH REWIND	90 IN/SEC
	SPEED VARIATION, SHORT TERM	$\pm$3%
	SPEED VARIATION, LONG TERM	$\pm$2%
	START/STOP PERIOD	$25/26 \times 10^{-3}$ SEC
	START/STOP DISTANCE	
	@ READ WRITE SPEED	0.300/0.405 INCHES
	@ SEARCH REWIND SPEED	2.97/3.42 INCHES
III.	POWER:	
	SERVO	+24 +15% @ [illegible]
	OTHER	$\pm$5 $\pm$4% VDC @ 1.6A TYP
	DISSIPATION: TYPICAL	18 WATTS
	MAXIMUM	69 WATTS
IV.	PHYSICAL: *	
	OVERALL WIDTH X HEIGHT X DEPTH	6.96 x 4.25 x 5.72 INCHES
	WEIGHT	4.2 LBS
	SIGNAL I/O MATING CONNECTOR	3M: 3425-3000
	POWER I/O MATING CONNECTOR	CANNON: 121-7326-10843 AND CANNON: 121-7326-702 WITH CONTACTS 11-0238-0091, KEYS 225-7301-003

V.	ENVIRONMENT:	
	OPERATING TEMP	6 TO 45°C
	STORAGE TEMP	-30 TO +60°C
	RELATIVE HUMIDITY	20 TO 80% RH
VI.	MACHINE RELIABILITY:	
	MEAN TIME BETWEEN FAILURES	> 3000 HOURS
	MEAN TIME TO REPAIR	<1.0 HOURS

ELECTRICAL SPECIFICATIONS

Power Supply Requirements

The voltages and corresponding current requirements for the Drive are listed in the below table.

POWER / DRIVE TYPE	DRIVE POWER DISSIPATION, WATTS		OPERATING CONDITIONS*	CURRENT REQUIREMENTS IN AMPERES (TOLERANCES INCLUDE RIPPLE					
				+24VDC ± 15%		-24VDC ± 15%		+5VDC+5%-3%	
				AMPS		AMPS		AMPS	
	TYP.	MAX.		TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
BASIC MODEL	15	53	1	0.1	0.1	0.2	0.3	0.4	0.9
			2	0.1	0.1	1.0	1.9	0.4	0.9
			3	0.9	1.7	0.2	0.3	0.4	0.9
			4	1.6	3.1	1.7	3.5	0.4	0.9
BASIC MODEL WITH A CONTROL BOARD	17	67	1	0.1	0.1	0.2	0.3	0.9	1.8
			2	0.1	0.1	1.0	1.9	1.0	2.0
			3	0.9	1.7	0.2	0.3	1.0	2.0
			4	1.6	3.1	1.7	3.5	1.0	2.0
BASIC MODEL WITH A CONTROL AND CODEC BOARD	18	69	1	0.1	0.1	0.2	0.4	1.2	2.4
			2	0.1	0.1	1.0	2.0	1.3	2.6
			3	0.9	1.7	0.2	0.4	1.3	2.6
			4	1.6	3.1	1.8	3.5	1.3	2.6

*Operating Conditions:
1. No tape motion, no write current.
2. Forward tape motion at 30 or 90 ips (includes writing conditions at 30 ips).

3. Reverse tape motion at 30 or 90 ips (no write current).
4. Start/Stop Periods: 30 ips 25/26 mSec., 90 ips 71/74 mSec.

General:
- All voltages measured at drive power connector.
- The ramp period current peaks do not occur simultaneously. A defective cartridge can extend ramp current periods.

Assumption for power dissipation calculations:
Typical: Nominal voltages and typical currents, 2 starts and 2 stops per second, and running 50% of the remaining time.
Maximum: Nominal voltages and maximum currents and 17 starts and 17 stops per second.

Interface Requirements for Basic Model Drives

Control and Status Interface

The interface between the Drive and the controller is single ended, TTL compatible, except for the data signals.

All input and output lines except data are defined as true low (0 to .8 VDC), and all Drive output lines are driven by an open collector or tri-state driver (25 ma maximum sink current). Input lines into the Drive supply various 74XX gates.

Proper line termination is required and subject to the exact cable used.

Data Signal Interface

The data signals, (Read Data and Write Data), are differential type. The Read Data signals (RDA+, RDA- and DAD+, DAD-) are driven by a SN 75110, or similar differential driver and the Write Data signals (WDA+, WDA-) are received by a differential receiver type LM 360 or similar. The data signal are designed for balanced transmission line operation and line termination within the Drive is optional.

The signal specification voltage swing shall be at least +50 mv but shall not exceed +3v, assuming a properly terminated line is being driven/received. The current to be sourced by the driver is 6.5 t1 15 ma/leg. The recommended termination will vary with the characteristic impedence of the cable as used. The maximum signal rise or fall time is 50 nsec.

Tape Motion, Starting and Stopping

The start distance is defined as the period from application of the state (either forward or reverse) command to when ≥95% of final long term speed is reached, exclusive of short term speed changes. For values of start distances, refer to the below table.

The minimum stopping distance shall always be greater than the maximum starting distance for 30 ips. An interrecord gap of 1.2 inches (3.048 cm) shall be achievable for 30 ips. A delay of 33 x 10^{-3} sec is required during writing to assure a minimum 1.2 inch interrecord gap. The delay is starting at the beginning of the Forward command.

The stop distance is the actual tape distance traveled during the stop period. During the stop period, which begins when the Drive motion is set false, the tape shall stop.

NOMINAL SPEED IN./SEC. (CM/SEC.)	CONDITION	PERIOD ($\times 10^{-3}$ SEC.	DISTANCE MIN. IN. (CM)	DISTANCE NOM. IN. (CM)	DISTANCE MAX. IN. (CM)
30 (76.2)	STARTING	25	.280 (.711)	.300 (.762)	.316 (.803)
	STOPPING	26	.378 (.960)	.405 (1.209)	.525 (1.334)
90 (228.6)	STARTING	71	2.701 (6.860)	2.979 (7.644)	3.201 (8.130)
	STOPPING	74	2.792 (7.092)	3.420 (8.687)	4.088 (10.38)

INTERFACE DESCRIPTION

I/O Signals for Basic Model Drives

Input Signals

SL2-, SL1-: Up to two Drives can share a common buss; drive is selected by either signal depending on internal address which must be specified. The Drive will not return status nor accept commands unless selected, except as specified below.

WEN-: When true, shall enable the writing and erasing functions for the selected track. The writing and erasing processes shall occur only if the cartridge is in the unprotected state (not safe). This signal will remain set after deselection. This signal should not be reset until the drive has stopped. This signal should be set prior to drive motion. At least 2 milliseconds should be allowed between the reset of Write Enable and the changing of the track select signals.

WDA-, WDA+: This signal will modulate the write head to produce a recorded wavefor- on tape when WEN- is true and the cartridge is in the unprotected state (not safe). This signal shall continue to modulate the write head if WEN is set and the cartridge is not protected independent of the drive selection.

To change to a WDA+=H, WDA-=L state shall cause a comparable change to be made on the RDA signal lines when read back.

The minimum clock period for data input should not allow the nominal resultant number of flux reversal from exceeding 6400 per inch (2520 flux reversal/cm).

FWD-:* Causes forward tape motion; the speed is set by the High Speed signal.

REV-:* Causes reverse tape motion; the speed is set by the High Speed signal.

HSP-: Causes the tape to move at High Speed in the direction set by FWD or REV.

TR2-, TR1-: Track select address: a binary number, (true low), in the following form:

2^1 2^0

Where 2^1 is TR2- and 2^0 is TR1-.

The track selection is decoded as follows:

ANSI Track Number	TR2- 2^1	TR1- 2^0
1	H	L
2	L	H
3	L	L
4	H	H

*: Simultaneous FWD & REV = True shall not cause damage to the drive but tape motion resulting is unpredictable.

The track selection will select all heads for a given track (i.e., erase, write, and read). The last track selection shall be stored within the drive even after deselection by the controller.

Output Signals

FIP-: The cartridge installed sensed by CIP is protected, i.e., cannot be written on under any operational conditions.

BLB-: Power is applied to Drive (+5VDC present) and sensor bulb is drawing current (is on).

LTH-, UTH-: Either upper (UTH) or lower (LTH) hole has been sensed. These signals are true for period of sensor activity ($\geq$100 µsec.) only.

CIP-: Cartridge is installed in Drive.

RDA+, RDA-: This signal is a replica of the WDA data written onto the tape except as specified herein.

The read signal is always available. The read signal lines should only be examined for valid data when DAD is true (low).

DAD+, DAD-: This signal, Data Detected, will indicate that the Read Data signals are valid for the particular mode of operation. The Read Data signals should be only examined when DAD is true. DAD will go true $\leq$16 µsec. after the first valid data transition is read from tape. This will remain true if at least two data transitions which exceed the threshold criteria are read from tape in the 16 µsec. period.

The DAD signal will remain true for up to 62 µsec. after the last data transition is read from a block, (the data transitions which have met the threshold criteria).

The DAD true state shall be DAD+ = High, DAD- = Low.

POWER - SIGNAL PIN ASSIGNMENTS

Power Connections

The power pin assignments for all Drive configurations are shown in the below table. Additional power connections for Drives with control and Codec Boards are shown in the next table.

Power Supply Pin Assignments

Pin #	Signal	From	Comments
1	M.N.C.	N.A.	Keying Plug
2	V24+	Power Supply	+24VDC
3	V24-	Power Supply	-24VDC
4	M.N.C.	N.A.	Keying Plug
5	SCOM	Power Supply	Servo Common
6	V5+	Power Supply	+5VDC
7	LCOM	Power Supply	Logic Common
8	CCOM	Drive	Chassis Common
9	M.N.C.	N.A.	
10	V24+	Power Supply	+24VDC
11	V24-	Power Supply	-24VDC
12	M.N.C.	N.A.	Keying Plug
13	SCOM	Power Supply	Servo Common
14	V5+	Power Supply	+5VDC
15	LCOM	Power Supply	Logic Common
16	CCOM	Drive	Chassis Common

Signal - Pin Assignments for Basic Model Drives

Pin #	Signal	From	Comments
1	SL2-	Controller	Select Unit 2
3	SL1-	Controller	Select Unit 1
5	FIP-	Drive	File Protected
7	BL2-	Drive	Bulb
9	LTH-	Drive	Lower Tape Hole
11	CIP-	Drive	Cartridge in Place
13	UTH-	Drive	Upper Tape Hole
15	RDA+	Drive	Read Data 1
16	RDA-	Drive	Read Data 2
17	LCOM	Drive	Logic Common
19	DAD+	Drive	Data Detected 1
20	DAD-	Drive	Data Detected 2
21	LCOM	Drive	Logic Common
23	TR1-	Controller	Track 2^0
25	TR2-	Controller	Track 2^1
27	M.N.C.	N.A.	
29	WDA+	Controller	Write Data 1
30	WDA-	Controller	Write Data 2
31	WEN-	Controller	Write Enable
33	M.N.C.	N.A.	
35	FWD-	Controller	Forward
37	REV-	Controller	Reverse
39	HSP-	Controller	High Speed

Notes:

1) All not listed ($2N \leq N \leq 20$) signal lines are the returns or grounds.

2) Mating connector is 3M Co. Part Number 3417-3000 or equivalent.

3) The above refers to Drives without a control board; connections are made directly to interconnect card.

4) M.N.C. Make no external connection.

APPENDIX B

DATA ACQUISITION ROUTINE

ADDRESS	DATA OR INSTRUCTION	LABEL	MNEMONIC	COMMENT
0A	05		ENI	ENABLE EXTERNAL INTERRUPT
B	25		EN TLNT I	ENABLE COUNTER INTERRUPT
C	85		CLR F0	CLEAR F0
D	A5		CLR F1	CLEAR F1
E	B5		CPL F1	SET F1=1
F	9ABF		ANL P2,#BFH	ENABLE TOTD INPUT
11	09		IN A,P1	INPUT TOTD
12	9615		JNZ (5)	IF NOT ZERO JMP
14	95		CPL.F0	IF ZERO SET CONTINUOUS FLAG
15	AB	(5)	MOV R3,A	STORE TOTD IN R3
16	89FF		ORL P1,#FFH	RESET P1
18	8AFF		URL P2,#FFH	RESET P2
1A	27		CLRA	INITIALIZE
1B	A8		MOV R0,A	ADDRESS ANT
1C	62		MOV T,A	COUNTER
1D	45		STRT CNT	START COUNTER
1E	BC10	(3)	MOV R4,#10H	INITIALIZE PAGE
20	CC	(2)	DEG R4	GET PAGE
21	FB		MOV A,R3	COMBINE PAGE
22	47		SWAP A	TMP SELECT
23	53F0		ANL A,#FOH	
25	43E0		URL A,#FOH	
27	4C		URL A,RY	
28	39		OUT2 P1,A	OUTPUT PAGE AND SELECT
29	7629	(1)	JF1 (1)	WAIT LOOP
2B	B5		LLP F1	RESET FLAG
2C	F8		MOV A,R0	TEST ADDRESS
2D	9629		JNZ (1)	IF NOT END OF PAGE JMP
2F	FC		MOV A,R4	IF END OF PAGE TEST
30	9620		JNZ (2)	FOR END OF BLOCK IF NOT END TMP
32	9ADF		ANL P2,#DF	IF END OF BLOCK RESET CPU2
34	BD00		MOV R5,#00H	WAIT FOR RESET
36	BE08		MOV R6,#08H	TO BE COMPLETED
38	ED38	(8)	DTNZ R5, (8)	
3A	EE38		DTNZ R6, (8)	
3C	8AFF		ORL P2,#FFH	
3E	CB		DEC R3	
3F	B61E		JFO (3)	IF CONTINUOUS FLAG IS SET JUMP
41	FB		MOV A,R3	TEST FOR END OF INTERVAL
42	961E		JNZ (3)	IF NOT END TMP
44	9A7F		ANL P2,#7FH	IF END RESET TIMER
46	8AFF		ORL P2,#FFH	AND SHUT DOWN
48				

```
                    L
          DATA OR   B
ADDRESS   INSTRUCTION L MNEMONIC        COMMENT

                        COUNTER INTERRUPT SERVICE ROUTINE

     50   9ADF           ANL P2,#DFH     START CONVERSION
     52   8AFF           ORL P2,#FFH
     54   93             RETR

                        EXTERNAL INTERRUPT SERVICE ROUTINE

     56   C8             DEC R0          SET ADDRESS
     57   90             MOVX,GRD,A      STORE DATA
     58   A5             CLR F1          CLEAR WAIR FLAG
     59   93             RETR


     83   91             RETR
```

WRITE TO TAPE ROUTINE

ADDRESS	DATA OR INSTRUCTION	LABEL	MNEMONIC	COMMENT
10	85		CLR F0	CLEAR FLAG 0
11	A5		CLR F1	CLEAR FLAG 1
12	05		ENI	ENABLE EXTERNAL INTERRUPT
13	BA10		MOV R2,#10H	INITIALIZE PAGE
15	B8FF		MOV R0,#FFH	INITIALIZE ADDRESS
17	9AFB		ANL P2,#FBH	ENABLE READ FOR TRACK & BLOCK CNT
19	09		IN A,P1	INPUT BLOCK COUNT (BLK CNT)
1A	A9		MOV R1,A	STORE IN R1
1B	C61E		JZ 500	IF ZERO JUMP
1D	95		CLP R0	IF NOT ZERO F0=1
1E	0A	500	1NA,P2	INPUT TRACK & MSB OF BLK CNT
1F	53F0		ANL A,#F0H	ZERO LOWER FOUR BITS
21	8AFF		URL P2,#FFH	RESET PORT2
23	89FF		URL P1,#FFH	RESET PORT1
25	AC		MOV R4,A	STORE TRK&MSB OF BLK CNT 1NR4
26	F247		JB7 100	JMP IF MSB OF BLK CNT IS 1
28	9656		JNZ 600	JMP IF TRK&BLK CNT IS NOT ZERO
2A	B656		JF0 600	JMP IF F0 SET FROM 1D ABOVE
2C	9AEF		ANL P2,#EFH	IF ZERO SET TRK 1 FOR STOP
2E	99EF		ANL P1,#EFH	AMD SELECT DATA REWRDER
30	9A6F		ANL P2,#GFH	START TAPE FORWARD
32	A5	200	CLR F1	CLEAR F1 FROM INT ROUTINE
33	3633	101	JTO 101	WAIT FOR UPPER TAPE HOLE
35	7632		JF1 200	JMP IF F1 IS SET FROM INT ROUTINE
37	BB70		MOV R3,#70H	ALLOW 4.8" DF TAPE
39	BE00		MOV RG,#00H	FROM LOAD POINT HOLE
3B	EE3B	102	DJNZ R6,102	
3D	EB3B		DJNZ R3,102	
3F	8ACF		URL P2,#CFH	STOP TAPE
41	BCAF		MOV R4,#AFH	STORE TRK1&MSB OF BLK CNT
43	B95E		MOV R1,#5EH	STORE BLOCK COUNT
45	0468		JMP 105	JMP TO 105
47	D2F3	100	JB6 118	IF NOT ZERO FROM INPUT TEST
49	00		NOP	FOR B7&B6 SET FOR END FLAG
4A	00		NOP	IF SET JMP TO "END" 118
4B	F9		MOV A,R1	GET BLK COUNT
4C	D35F		XRL A,#5EH	TEST FOR FIRST WRITE OF TRK
4E	9656		JNZ 600	IF NOT FIRST WRITE TMP TO 600
50	FC		MOV A,R4	IF FRST WRITE GET TRK

ADDRESS	DATA OR INSTRUCTION	L B	MNEMONIC	COMMENT
51	43CF		URL A,#CFH	SET FOR STOP
53	3A		OUTL P2,A	OUTPUT TO DATA RECORDER
54	0468		TMP 105	TMP TO 105
56	FC	600	MOV A,R4	IF NOT FIRST WRITE OF TRK GET TRK
57	43CF		URLA,#CFH	AND SET FOR STOP
59	3A		OUTL P2,A	OUTPUT TRK TO DA.A RECORDER
5A	9ABF		ANL P2,#BEH	START REVERSE RUN
5C	465C	106	JNT1 100	WAIT FOR DAD+TO 00 TRUE
5E	8ACF		URL P2,#CFH	STOP TAPE
60	9A7F		ANL P2,#7FH	START TAPE FORWARD
62	5662	107	JT1 107	WAIR FOR DAD&TO 00 FALSE
64	8ACF		URL P2,FCFH	STOP TAPE
66	BD60	105	MOV R5,#60H	SET MASK FOR WEN-&PAGE
68	997F		ANL P1,#7FH	SET WRITE ENABLE(WEN-)
6A	9A7F		ANL P2,#7FH	START TAPE FORWARD
6C	BB21		MOV R3,#21H	WAIT FOR 1.2" INTER BLOCK
6E	BE00		MOV R6,#00H	GAP TO GO BY
70	EE70	108	DTNZ R6, 108	
72	EB70		DTNZ R3, 108	
74	9AF7		ANL P2,#F7H	TRIGGER SHIFT REG&MFM ENCODER
76	8AFF		URL P2,#0FH	RESET TRIGGER
78	BB40		MOV R3,#4DH	WAIT FOR PREAMBLE "0's"
7A	EB7A	109	DTNZ R3,109	
7C	99DF		ANL P1,#DFH	TRIGGER PREAMBLE "1"
7E	BB02		MOV R3,#02H	DELAY 12 INSTRUCTION
80	EB8D	110	DJNZ R3,110	CYCLES FOR 1 TO SHIFT THRU
82	CA	2	DEC R2	GET PAGE
83	FD		MOV A, R5	GET MASK
84	DA		XRL A, R2	COMBINE PAGE AND MASK
85	39		OUTL P1,A	OUTPUT PAGE
86	80	1	MOVX A,@R0	WRITE TO SHIFT REGISTER
87	238A		MOV A,#8A	DELAY INSTRUCTION CYCLES
89	B3		JMPP @A	
8A	00	111	NOP	
8B	BB01		MOV R3,#01H	
8D	EB8D	112	DTNZ R3, 112	
8F	E886		DTNZ R0, 1	DEC ADDRESS IF NOT ZERO JMP 1
91	80		MOVX A,@R0	IF ZERO GET LAST ADDR OF PAGE
92	0494		JMP 112	DELAY
94	C8	113	DEC R0	INITIALIZE ADDRESS FOR NEW PAGE

ADDRESS	DATA OR INSTRUCTION	LBL	MNEMONIC	COMMENT
95	FA		MOV A,R2	TEST FOR LAST PAGE
96	9682		JNZ (2)	IF NOT LAST PAGE JMP TO 2
98	BB4D		MOV R3,#4DH	IF LAST PAGE ALLOW POSTAMBLE
9A	EB9A	(114)	DJNZ R3,(114)	
9C	8ACF		URL P2,#CFH	STOP TAPE
9E	897F		URL P1,#7FH	DELECT DATA RECORDER
A0	89FF		URL P1,#FFH	DISABLE WRITE (WEN-)
A2	C9		DEC R1	DECREMENT BLOCK COUNT
A3	F9		MOV A,R1	GET BLK CNT
A4	96F3		JNZ (118)	IF NOT ZERO JMP TO (118)
A6	F6		MOV A,R4	IF ZERO GET MSB OF BLK CNT
A7	F2AE		JB7 (400)	IF B0 IS SET JMP TO (400)
A9	D2B3		JB6 (401)	IF B8 BUT NOT B9 SET JMP TO (401)
A0	04B7		JMP (117)	IF TRK IS FULL JMP TO (117)
AD	D360	(400)	XRL A,#COH	IF B9 IS SET CLEAR B9 & SET B8
AF	AC		MOV R4,A	STOP NEW BLOCK CNT W/VLD TRK
B0	04F3		JMP (118)	JMP TO (118)
B2	533F	(401)	ANL A,#3FH	IF B9 NOT SET & B8 SET CLEAR B8
B4	AC		MOV R4,A	STORE NEW BLK CNT W/OLD TRK
B5	04F3		JMP (118)	JMP TO (118)
B7	B2C1	(117)	JB5 (120)	IF TRK FULL TEST TRK CODE FOR
B9	92CD		JB4 (130)	NEW TRK
BB	BCBF		MOV R4,#BFH	IF TRK 3, SET TRK 4 AND
BD	B95E		MOV R1,#5EH	NEW BLOCK COUNT
BE	04D1		JMP (121)	JMP (121) REWIND
C1	92C9	(120)	JB4 (119)	TEST FOR TRK 1
C3	BC9F		MOV R4,#9FH	IF TRK1, SET TRK2 AND NEW
C5	B95E		MOV R1,#5EH	BLOCK COUNT
C7	04D1		JMP (121)	JMP (121) REWIND
C9	BCFF	(119)	MOV R4,#FFH	IF TRK 4 SET FLAG FOR END OF
CB	04F3		JMP (118)	TAPE AND JMP TO STORE
CD	BC8F	(130)	MOV R4,#8FH	IF TRK 2, SET TRK 3 AND NEW
CF	B95E		MOV R1,#5EH	BLOCK COUNT
D1	99EF	(121)	ANL P1,#EFH	SELECT DATA RECORDER
D3	F6		MOV A,R4	GET TRK
D4	43CF		URL A,#CFH	SET FOR STOP
D6	3A		OUTL P2,A	OUTPUT TRK TO DATA RECORDER
D7	99AF		ANL P1,AFH	SET FOR HIGH SPEED
D9	9ABF		ANL P2,BFH	START REWIND
DB	BB20		MOV R3,#20H	WAIT FOR EARLY WARNING
DD	EBDD	(122)	DJNZ R3,(122)	HOLE TO PASS

```
                    L
          DATA OR   B
ADDRESS   INSTRUCTION L MNEMONIC        COMMENT

     DF   36DF       123 JTD 123        WAIT FOR LOAD POINT HOLE
     E1   8ACF           URL P2,#CFH    STOP TAPE
     E3   89EF           URL P1,#EFH    DISABLE HIGH SPEED
     E5   9A7F           ANL P2,#7FH    START TAPE FORWARD
     E7   36E7       124 JTO 124        WAIT FOR LOAD POINT HOLE
     E9   BB7D           MOV R3,#7DH    ALLOW FOR 4.8" TO PASS
     EB   BE0D           MOV R6,#00H    AFTER LOAD POINT HOLE
     ED   EEED       125 DJNZ R6, 125
     EF   EBED           DJNZ R3, 125
     F1   8ACF           URL P2,#CFH    STOP TAPE
     F3   89FF       118 URL P1,#FFH    DESELECT DRIVE
     F5   8AFF           URL P2,#FFH    RESET P2
     F7   9AFD           ANL P2,#FDH    ENALBE WRITE
     F9   F9             MOV A,R1       GET BLOCK COUNT
     FA   39             OUT2 P1,A      OUTPUT BLOCK COUNT TO P1
     FB   FC             MOV A,R4       GET TRK
     FC   53F0           ANLA,#FDH      MASK LOWER 4 BITS
     FE   3A             OUTL P2,A      OUTPUT TRK TO P2
     FF   9AF5           ANL P2,#F5H    TRIGGER WRITE TO STORAGE
    101   89FF           URL P1,#FFH    RESET PORT1
    103   8AFF           URL P2,#FFH    RESET PORT2
    105   9AFE           ANL P2,#FEH    SHUT DOWN CPU2&DATA RECORDER
    107

                        INTERRUPT SERVICE ROUTINE

    120   3642           JTO 100        JMP IF UTH NOT PRESENT
     22   9226           JB4 101        IF TRK 2 OR 4 JMP
     24   823E           JB5 102        IF TRK 1 JMP
     26   8AL0       101 URL P2,#C0H    IF TRK 2,3 OR 4 STOP TAPE
     28   8940           URL P1,#40H    DESELECT HIGH SPEED
     2A   9A7F           ANL P2,#7FH    START TAPE FORWARD
     2C   2300           MOV R6,#10H    WAIT FOR 130T HOLES TO
     2E   EE2E       104 DJNZ R0,104    PASS
     30   3630       105 JTO 105        WAIT FOR LOAD PT HOLE
     32   BB7D           MOV R3,#7DH    ALLOW 4.8" AFTER LP HOLE
     34   BE00           MOV R6,#00H
     36   EE36       106 DJNZ R6,100
     38   EB36           DJNZ R3,100
     3A   8AC0           URL P2,#C0H    STOP TAPE
     3C   247E           JMP 120        JMP TO RETURN
     3E   A5         102 CLR F1         SET F1
     3F   B5             CPLF1
     40   247E           JMP 120        JMP TO RETURN
     42   8AC0       100 URL P2,#C0H    STOP TAPE
     44   B24E           JB5 120        IF END OF TRACK TEST
     46   925A           JB4 130        TRK CODE
     48   BCBF           MOV R4,#BFH    IF TRK3 SET TRK4 AND
```

ADDRESS	DATA OR INSTRUCTION	LBL	MNEMONIC	COMMENT
4A	B95E		MOV R1,#5EH	- BLOCK COUNT
4C	245E		JMP 121	JMP TO REWIND
4E	4256	120	JB4 119	IF TRK1 SET TRK2
50	BC9F		MOV R4,#9FH	-
52	B95E		MOV R1,#5EH	-
54	245E		JMP 121	JMP TO REWIND
56	BCFF	119	MOV R4,#FFH	IF TRK4 SET END OF TAPE
58	245E		JMP 121	FLAG & JMP TO REWIND
5A	BC8F	130	MOV R4,#8FH	-FF TRK2 SET TRK3 AND
5C	B95E		MOV R1,#5EH	BLOCK COUNT
5E	FC	121	MOV A,R4	GET TRACK
5F	43CF		URLA,#CFH	OUTPUT WITH STOP
61	3A		OUTL P2,A	
63	99AF		ANL P1,#AFH	SELECT HIGH SPEED
64	9ABF		ANL P2,#BFH	START REWIND
66	BB20		MOV R3,#20H	WAIT FOR EARLY WARNING
68	EB68	122	DJNZ R3,122	HOLE TO PASS
6A	366A	123	JTO 123	WAIT FOR LP HOLE
6C	8ACF		URL P2,#CFH	STOP TAPE
6E	897F		URL P1,#7FH	DESELECT HIGH SPEED
70	9A7F		ANL P2,#7FH	START TAPE FORWARD
72	3672	124	JTO 124	WAIT FOR LOAD POINT HOLE
74	BB7D		MOV R3,#7DH	ALLOW 4.8" AFTER LP HOLE
76	BE00		MOV R6,#00H	
78	EE78	125	DJNZ R6,125	
7A	EB78		DJNZ R3,125	
76	8ALF		URL P2,#LFH	STOP TAPE
7E	93	126	RETR	RETURN
7F				

D/A ROUTINE

ADDRESS	DATA OR INSTRUCTION	LABEL	MNEMONIC	COMMENT
A	9ABF		AN2 P2,#BF H	ENABLE INPUT OF TOTD
C	09		IN A,P1	INPUT TOTD
D	AB		MOV R3,A	STORE IN R3
E	9611		JNZ (90)	IF NOT ZERO JMP
10	B5		CPL F1	IF ZERO SET CONTINUOUS FLAG
11	89FF	(90)	URL P1,#FFH	RESET P1
13	8AFF		URL P2,#FFH	RESET P2
15	B800		MOV R0,#00H	INITIALIZE ADDRESS
17	B61D		MOV R4,#10H	INITIALIZE PAGE
19	FB		MOV A,R3	GET TOTD
1A	47		SWAP A	SET TOTD'S SLB
1B	43EF		URL A,#EFH	FOR SELECT TO MUX
1D	39		OUTL P1,A	OUTPUT TO MUX
1E	9ADF		ANL P2,#DFH	TRIGGER CPU2 FOR FIRST LOAD
20	BD08		MOV R5,#08H	DELAY FOR CPU2 TO
22	EE22	(101)	DJNZ R6,(101)	GET STARTED
24	ED22		DTNZ R5,(101)	
26	8AFF		URL P2,#FFH	RESTORE RESET
28	BD19		MOV R5,#19H	WAIT FOR FIRST WORD
2A	EE2A	(110)	DJNZ R6,(110)	TO BE COMPLETE
2C	ED2A		DJNZ R5,(110)	
2E	85	(3)	CLR F0	CLEAR NEW LOAD FLAG
2F	BC10		MOV R4,#10H	REINITIALIZE PAGE
31	CB		DEG R3	GET NEW SELECT
32	FB		MOV A,R3	
33	47		SWAP A	
34	53F0		ANL A,#FOH	
36	43E0		URL A,#EOH	
38	AF		MOV R7,A	
39	CC	(2)	DEC R4	GET NEW PAGE
3A	FF		MOV A,R7	COMBINE PAGE AND
3B	4C		URL A,R4	SELECT
3C	39		OUTL P1,A	OUTPUT PAGE AND SELECT
3D	B650		JFO (170)	JMP IF NEW LOAD FLAG SET
3F	FC		MOV A,R4	CHECK ON PAGE COMPLETE
40	D30E		XRL A,#OEH	AFTER TRIGGER TO CPU2
42	964A		JNZ (160)	IF NOT GO TO RESET OF CPU2
44	8AFF		URL P2,#FFH	IF ONE PAGE HAS PAST
46	95		CPL F0	RESTORE RESET & SET
47	00		NOP	NO LOAD FLAG
48	0455		JMP (1)	
4A	9ADF	(160)	ANL P2,#DFH	RESET CPU#2
4C	00		NOP	
4D	00		NOP	

ADDRESS	DATA OR INSTRUCTION	L B L	MNEMONIC	COMMENT
4E	0455		JMP (1)	START D/A CYCLE
50	00	(170)	NOP	DELAY
51	BE04		MOV R6,#04	
53	EE53	(180)	DJNZ R6,(180)	
55	C8	(1)	DEC R0	GET ADDRESS
56	80		MOVX A,@R0	1-D/A
57	F8		MOV A,R0	TEST FOR END OF PAGE
58	CG60		JZ (200)	
5A	BE14		MOV R6,#14H	IF NOT END DELAY
5C	EE5C	(220)	DJNZ R6,(220)	
5E	0455		JMP (1)	JMP FOR NEXT D/A
60	FC	(200)	MOV A,R4	TEST FOR LAST PAGE
61	CG6A		JZ (210)	IF LAST PAGE JMP
63	00		NOP	IF NOT LAST PAGE DELAY
64	BE09		MOV R6,#09H	
66	EE66	(230)	DJNZ R6,(230)	
68	0439		JMP (2)	JMP FOR PAGE RACE
6A	00	(210)	NOP	IF LAST PAGE DELAY
6B	BE03		MOV R6,#03H	
6D	EE6D	(240)	DJNZ R6,(240)	
6F	FB		MOV A,R3	TEST FOR LAST BLOCK
70	962E		JNZ (3)	IF NOT LAST BLOCK JMP
72	762E		JF1 (3)	IF LAST BLOCK
74	99BF		ANL P1,#BFH	SET SIGNAL
76	0476	(250)	JMP (250)	WAIR FOR RESET.

READ FROM TAPE

ADDRESS	DATA OR INSTRUCTION	LBL	MNEMONIC	COMMENT
8	05		ENI	ENABLE EXTERNAL INTERRUPT
9	BA10		MOV R2,#10H	INITIALIZE PAGE
B	B800		MOV R0,#00H	INITIALIZE ADDRESS
D	BDE0		MOV R5,#EOH	SET MASK
F	BCAF		MOV R4,#AFH	STORE TRK 1 AND BLOCK
11	B95E		MOV R1,#5EH	COUNT
13	FC		MOV A,R4	GET TRACK
14	43CF		ORLA,#CFH	SET TRACK FOR STOP
16	99EF		ANL P1,#EFH	SELECT DATA RECORDER
18	3A		OUTL P2,A	OUTPUT TRACK
19	9A7F		ANL P2,#7FH	START TAPE FORWARD
1B		200	CLR F1	CLEAR F1 FOR $\overline{INT}$ ROUTINE
1C	361C	101	JTO 101	WAIT FOR LOAD POINT HOLE
1E	761B		JF1 200	IF $\overline{INT}$ GO BACK TO WAITING FOR LP
20	8ALF		URL P2,#CFH	STOP TAPE AT LP HOLE
22	0428		JMP 105	JMP TO 105 FOR START READ
24	FC	100	MOV A,R4	GET OLD TRACK
25	43CF		ORLA,#CFH	SET FOR STOP
27	3A		OUTL P2,A	OUTPUT TRK TO DATA REORDER
28	9A7F	105	ANL P2,#7FH	START TAPE FORWARD
2A	262A	106	JNT1 106	WAIT FOR "1" OF PREAMBLE
2C	BB05		MOV R3,#03H	WAIT 8 INSTRUCTION CYCLES
2E	EB2E	107	DJNZ R3,107	
30	CA	2	DEC R2	GET PAGE
31	FD		MOV A,R5	GET MASK
32	DA		XRL A,R2	COMBINE PACE AND MASK
33	39		OUTL P1,A	OUTPUT PACE & MASK
34	90	1	MOV X@P0,A	READ FROM SHIFT REG
35	DB09		MOV R3,#09H	WAIT 20 INSTRUCTION CYCLES
37	EB37	108	DJNZ R3,108	
39	EB34		DJNZ R0,1	DEC. ADDR IF NOT ZERO JMP TO1
3B	4D		MOV X @R0,A	IF ZERO READ LAST OF PAGE
3C	C8		DEC R0	RESET PACE ADDRESS
3D	00		NOP	USE UP 13 INSTRUCTION
3E	BB05		MOV R3,#05H	CYCLES
40	EB40	104	DTNZ R3,104	
42	EA		MOV A,R2	GET PAGE
43	9630		JNZ 2	IF NOT LAST PAGE JMP TO 2
45	8ACF		URL P2,#CFH	IF LAST PAGE STOP TAPE
47	897F		URL P1,#7FH	DESELECT DATA RECORDER

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ADDRESS	DATA OR INSTRUCTION	LBL	MNEMONIC	COMMENT
49	L9		DECR1	DEC BLOCK COUNT
4A	F9		MOV A,R1	TEST BLK CNT FOR
4B	968E		JNZ (118)	ZERO
4D	FC		MOV AIR4	IF NOT ZERO GET TRR
4E	F254		JB7 (400)	IF MOD OF BLK CNT IS SET JMP (400)
50	D259		JB6 (401)	IF B8 OF BLK CNT IS SET JMP TO (401)
52	045E		JMP (117)	IF NEITHER IS SET GET NEW TRK
54	D3C0	(400)	XRL A,#COH	IF MSB OF BLK COUNT IS SET
56	AC		MOV R4,A	SET B9 AND STORE
57	048E		JMP (118)	JMP TO (118) STOP
59	533F	(401)	ANL A,#3FH	IF B9 IS NOT SET BUT B8 IS SET
5B	AC		MOV R4,A	CLR B8 AND STORE
5C	D48E		JMP (118)	JMP TO (118) STOP
5E	B268	(117)	JB5 (120)	IF END OF TRK TEST TRK CODE
60	9274		JB4 (130)	FOR NEXT TRK
62	BCBF		MOV R4,#BFH	IF TRKS SET TRK 4 AND
64	B95E		MOV R1,#5EH	BLOCK COUNT
66	0478		JMP (121)	JMP TO REWIND
68	9270	(120)	JB4 (119)	IF TRK 1 SET TRK 2
6A	BC9F		MOV R4,#9FH	AND BLOCK COUNT
6C	B95E		MOV R1,#5EH	
6E	0478		JMP (121)	JMP TO REWIND
70	BCFF	(119)	MOV R4,#FFH	IF TRK 4 SET END OF TAPE
72	0494		JMP (125)	FLACE & JMP TO END LOOP
74	BC8F	(130)	MOV R4,#8FH	IF TRK 2 SET TRK 3 AND
76	B95E		MOV R1,#5EH	BLOCK COUNT
78	99EF	(121)	ANL P1,#EFH	SELECT DATA RECORDER
7A	FC		MOV A,R4	GET TRACK
7B	43CF		URL A,#CFH	SET TRACK FOR STOP
7D	3A		OUTL P2,A	OUTPUT TO DATA RECORDER
7E	99AF		ANL P1,#AFH	SET FOR HIGH SPEED
80	9A7F		ANL P2,#7FH	START REWIND
82	BB20		MOV R3,#20H	WAIT FOR EARLY WARNING
84	EB84	(122)	DJNZ R3,(122)	HOLE TO PASS
86	3686	(123)	JTO (123)	WAIT FOR LOAD POINT HOLE
88	8ACF		URL P2,#CFH	STOP TAPE
8A	89EF		URL P1,#EFH	RESET P1
8C	8AFF		URL P2,#FFH	RESET P2
8E	8AFF	(118)	URL P2,#FFH	RESET P2
90	5690	(124)	JT1 (124)	WAIT FOR TRIGGER FROM CPU1
92	0424		JMP (100)	WHEN TRIGGERED START FROM (100)
94	0494	(125)	JMP (125)	END OF TAPE LOOP

ADDRESS	DATA OR INSTRUCTION	L B L	MNEMONIC	COMMENT
0FF	FC		MOV A,R4	GET PRESENT TRACK
100	361A		JTO 100	JMP IF UTH NOT PRESENT
102	9206		JB4 101	IF TRK 2 OR 4 JMP
104	B216		JB5 102	IF TRK 1 JMP
106	8AC0	101	URL P2,#COH	IF TRK 2, 3 OR 4 STOP TAPE
108	8940		URL P1,#40H	DESELECT HIGH SPEED
10A	9A7F		ANL P2,#7FH	START TAPE FORWARD
10C	BF0D		MOV R6,#00H	TEST FOR LOAD PT HOLE
10E	EE0E	104	DJNZ R6,104	
110	3610	105	JTO 105	WAIT FOR LOAD PT HOLE
112	8AC0		URL P2,#CDH	STOP TAPE
114	2448		JMP 126	JMP TO RETURN
116	A5	102	CLR F1	SET F1
117	B5		CPL F1	
118	2448		JMP 126	JMP TO RETURN
11A	8AC0	100	URL P2,#COH	STOP TAPE
11C	B226		JB5 120	IF END OF TRACK TEST
11E	9232		JB4 120	TRACK CODE
120	BC70		MOV R4,#70H	IF TRK 3 SET TRK 4
122	B996		MOV R1,#96H	AND BLOCK COUNT
124	2436		JMP 121	JMP TO REWIND
126	922E	120	JB4 119	IF TRK 1 SET TRK 2
128	BC50		MOV R4,#50H	AND BLOCK COUNT
12A	B996		MOV R1,#96H	
12C	2436		JMP 121	JMP TO REWIND
12E	BCF0	119	MOV R4,#FOH	IF TRK 4 SET END OF
130	2448		JMP 126	TAPE FLAG JMP TO RETURN
132	BC40	130	MOV R4,#40H	IF TRK 2 SET TRK 3
132	B996		MOV R1,#96H	AND JMP TO RETURN
136	FC	121	MOV A,R4	GET TRACK
137	43CF		URL A,#CFH	OUTPUT AT STOP
139	3A		OUTL P2,A	
13A	99AF		ANL P1,#AFH	SELECT HIGH SPEED
13C	9ABF		ANL P2,#BFH	START REWIND
13E	BB20		MOV R3,#20H	ALLOW EARLY WARNING
140	EB40	122	DJNZ R3,122	HOLE TO PASS
142	3642	123	J TO 123	WAIT FOR LP HOLE
144	8ACF		URL P2,#CFH	STOP TAPE
146	89EF		URL P1,#EFH	DESELECT HIGH SPEED
148	93	120	RETR	RETURN

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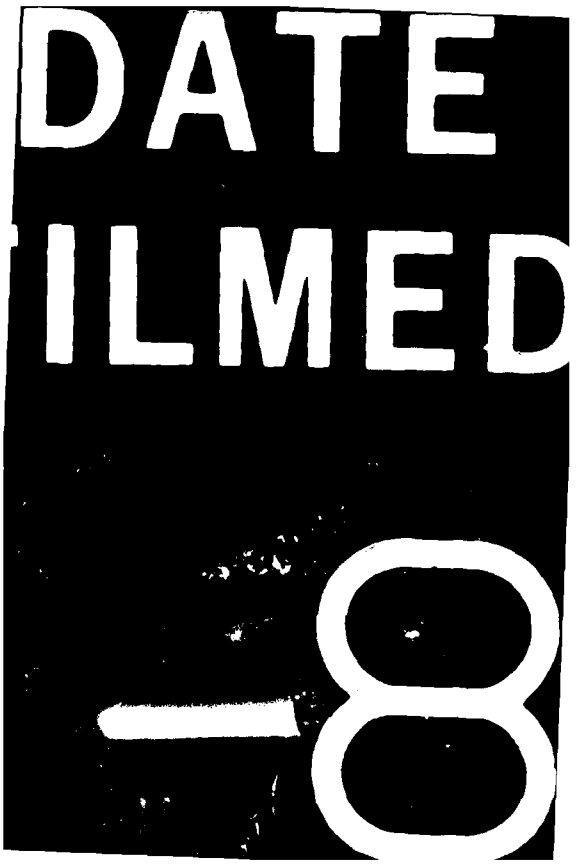
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